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2) Select the fields to search for each keyword.
3) Select search operators when using multiple keywords.
4) Limit the results by selecting Search Options.
5) Click Search. See Search Examples

pulse code In: All Fields

And

multipath In: All Fields

And

propagation In: All Fields

Search Clear

Note: This function returns plural and suffixed forms of the keyword(s).

Search Options:
Select publication types:

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- [x] IEE Journals
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3) Select search operators when using multiple keywords.
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5) Click Search. See Search Examples

pulse In: All Fields

And

code In: All Fields

And

propagation In: All Fields

Search Clear

Note: This function returns plural and suffixed forms of the keyword(s).

Search Options:
Select publication types:

- [x] IEEE Journals
- [x] IEE Journals
- [x] IEEE Conference proceedings
- [x] IEE Conference proceedings
- [x] IEEE Standards

Select years to search:

From year: All to Present

Organize search results by:

Sort by: Relevance
In: Descending order
List 15 Results per page

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	1	RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and (transmi$4 same code same (pulse-rate or pulse adj rate))	USPAT; US-PGPUB	2004/07/28 12:34			0
2	BRS	5	RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and (code same (pulse-rate or pulse adj rate))	USPAT; US-PGPUB	2004/07/28 12:38			0
3	BRS	40	RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and code	USPAT; US-PGPUB	2004/07/28 14:10			0
4	BRS	14	RF and (transmi$4 same (plurality or multiple) same pulse same multipath same propagation) and code	USPAT; US-PGPUB	2004/07/28 13:21			0
5	IS&R	1050	(375/130).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:07			0
6	IS&R	81	(375/135).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:07			0
7	IS&R	135	(375/136).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:07			0
8	IS&R	283	(375/140).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:08			0
9	IS&R	351	(375/141).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:08			0
10	IS&R	192	(375/145).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:08			0
11	IS&R	380	(375/146).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:09			0
12	IS&R	545	(375/147).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:09			0
13	IS&R	597	(375/242).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:09			0
14	IS&R	808	(375/295).CCLS.	USPAT; US-PGPUB; EPO; DERWENT	2004/07/28 14:10			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
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18	BRS	0	(RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and code) and ((375/145).CCLS.)	USPAT; US-PGPUB	2004/07/28 14:11			0
19	BRS	0	(RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and code) and ((375/146).CCLS.)	USPAT; US-PGPUB	2004/07/28 14:11			0
20	BRS	0	(RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and code) and ((375/242).CCLS.)	USPAT; US-PGPUB	2004/07/28 14:11			0
21	BRS	1	(RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and code) and ((375/316).CCLS.)	USPAT; US-PGPUB	2004/07/28 14:17			0
22	BRS	3	(RF and (transmi$4 same (plurality or multiple) same pulse same multipath) and code) and ((375/130).CCLS.)	USPAT; US-PGPUB	2004/07/28 14:12			0
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United States Patent [19]

Dunn et al.

[11] **Patent Number: 4,761,796**

[45] **Date of Patent: Aug. 2, 1988**

[54] **HIGH FREQUENCY SPREAD SPECTRUM COMMUNICATION SYSTEM TERMINAL**

[75] Inventors: **James Dunn**, San Diego, Calif.; **Charles Sanford**, Iselin; **Joseph Kadin**, Florham Park, both of N.J.

[73] Assignee: **ITT Defense Communications**, Nutley, N.J.

[21] Appl. No.: **694,549**

[22] Filed: **Jan. 24, 1985**

[51] **Int. Cl.**[4] **H04L 27/30**

[52] **U.S. Cl.** **375/1**; 380/34

[58] **Field of Search** 375/1, 107; 381/43; 380/34

[56] **References Cited**

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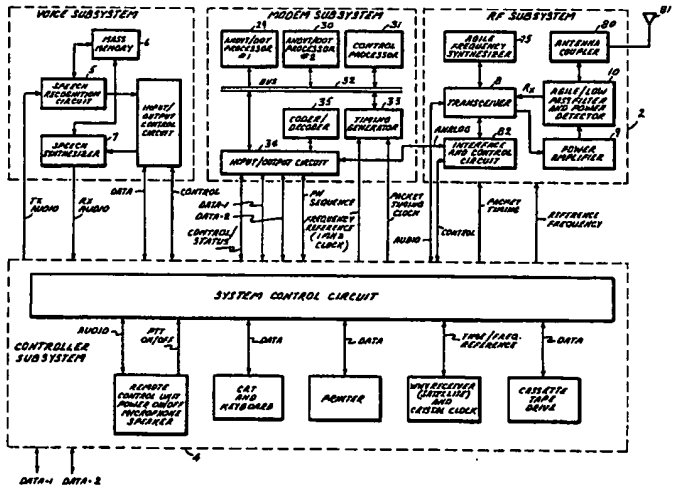
4,287,597	9/1981	Paynter et al.	375/107
4,435,822	3/1984	Spencer et al.	375/1
4,606,041	8/1986	Kadin	375/1

Primary Examiner—Cangialosi, Salvatore
Assistant Examiner—Aaron J. Lewis
Attorney, Agent, or Firm—Robert A. Walsh; Thomas N. Twomey; Mary C. Werner

[57] **ABSTRACT**

The spread spectrum communication system terminal comprises a first subsystem including a first arrangement to encode a locally generally digital data with an error correcting code, a second arrangement for spectrum spreading of the encoded locally generated digital data in at least one mode of operation of the communication system terminal, a third arrangement to receive remotely generated error correcting code encoded digitla data spectrum spread in the one mode of operation and a fourth arrangement to recover the remotely generated digital data. In addition, a second subsystem includes a fifth arrangement frequency hopping the encoded locally generated digital data prior to transmission to a remote location and a sixth arrangement frequency dehopping the encoded remotely generated digital data received from the remote location. A third subsystem is also provided including a seventh arrangement to provide a predetermined signal for spectrum spreading the encoded locally generated digital data in the one mode of operation and to couple the encoded locally generated digital data to the fifth arrangement and an eighth arrangement to provide a reference frequency for the frequency hopping and frequency dehopping and to couple the frequecny dehopped encoded remotely generated digital data from the sixth arrangement to the third arrangement.

8 Claims, 15 Drawing Sheets



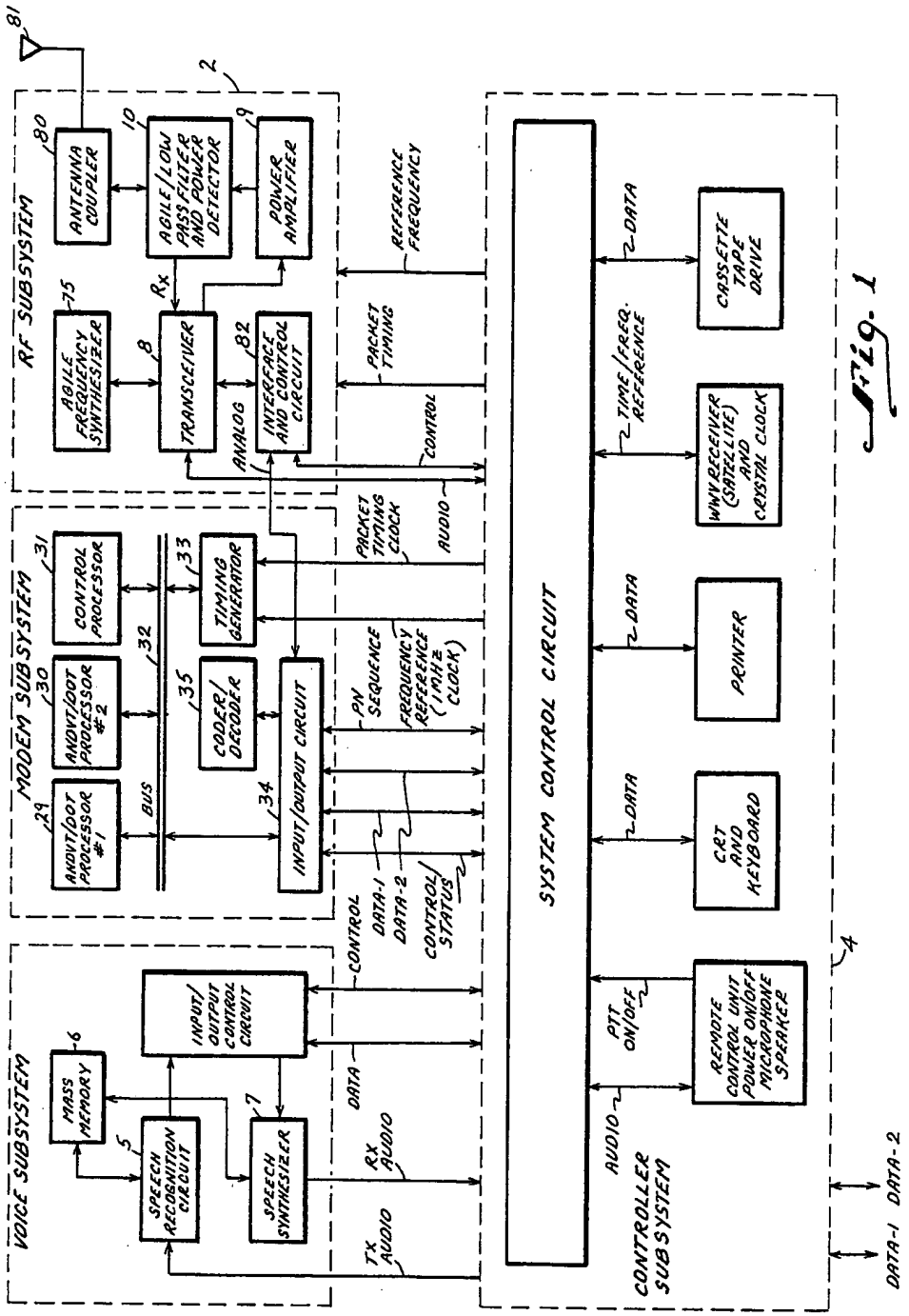

RF SUBSYSTEM
ANTENNA COUPLER
ABILE/LOW PASS FILTER AND POWER DETECTOR
POWER AMPLIFIER
ABILE FREQUENCY SYNTHESIZER
TRANSCEIVER
INTERFACE AND CONTROL CIRCUIT
REFERENCE FREQUENCY
PACKET TIMING
CONTROL
ANALOG
MODEM SUBSYSTEM
CONTROL PROCESSOR
TIMING GENERATOR
ANDVT/DOT PROCESSOR #2
CODER/DECODER
ANDVT/DOT PROCESSOR #1
INPUT/OUTPUT CIRCUIT
BUS
PACKET TIMING CLOCK
AUDIO
PN SEQUENCE
FREQUENCY REFERENCE (MINE CLOCK)
CONTROL
DATA-1
DATA-2
CONTROL STATUS
VOICE SUBSYSTEM
MASS MEMORY
INPUT/OUTPUT CONTROL CIRCUIT
SPEECH RECOGNITION CIRCUIT
SPEECH SYNTHESIZER
DATA
RX AUDIO
TX AUDIO
SYSTEM CONTROL CIRCUIT
CONTROLLER SUBSYSTEM
PTT ON/OFF
AUDIO
2-DATA
TIME/FREQ. REFERENCE
CASSETTE TAPE DRIVE
WWV RECEIVER (SATELLITE) AND CRYSTAL CLOCK
PRINTER
CRT AND KEYBOARD
REMOTE CONTROL UNIT POWER ON/OFF MICROPHONE SPEAKER
DATA-1 DATA-2

FIG. 1

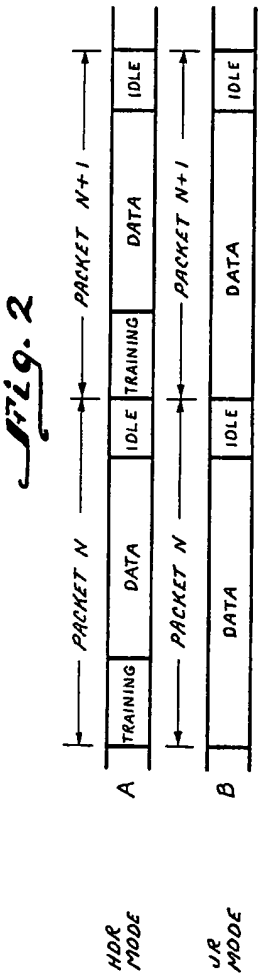


Fig. 2

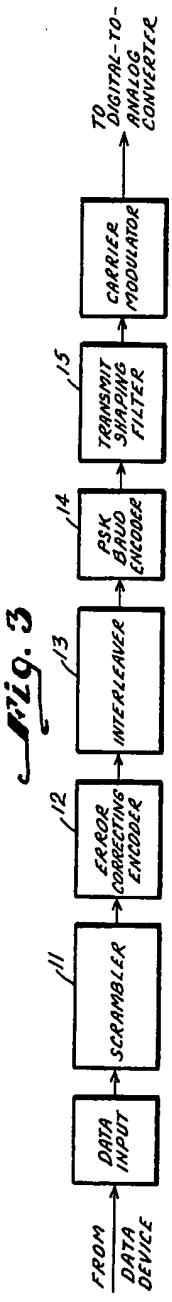


Fig. 3

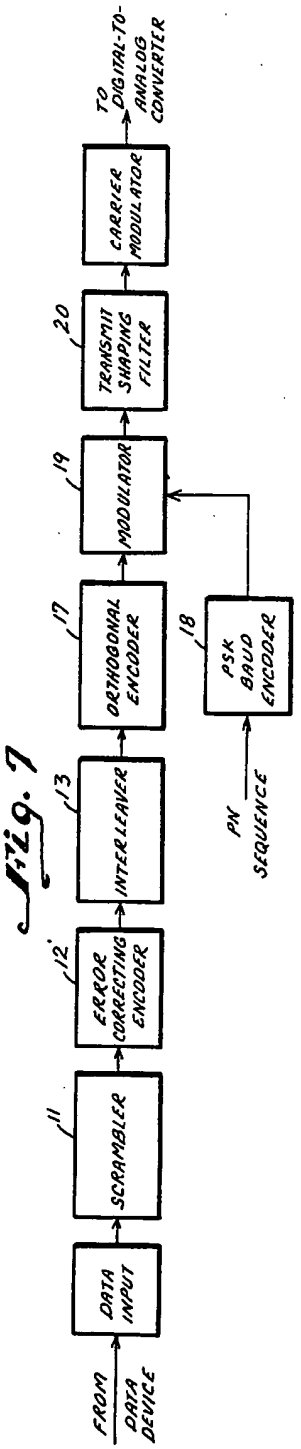


Fig. 7

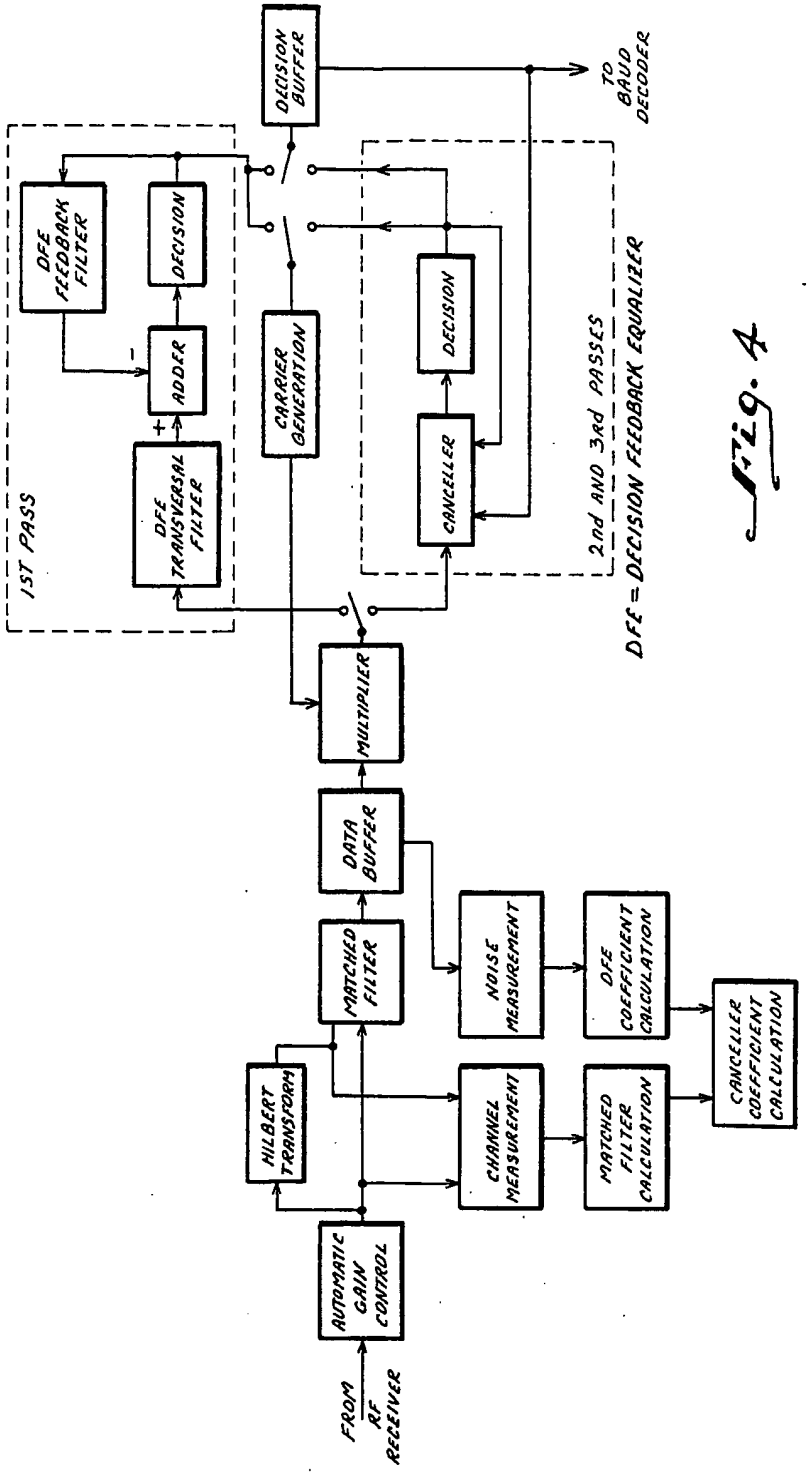

DECISION BUFFER
TO BAUD DECODER
DFE FEEDBACK FILTER
DECISION
ADDER
DFE TRANSVERSAL FILTER
CARRIER GENERATION
DECISION
CANCELLER
1ST PASS
2nd AND 3rd PASSES
DFE = DECISION FEEDBACK EQUALIZER
MULTIPLIER
DATA BUFFER
MATCHED FILTER
NOISE MEASUREMENT
DFE COEFFICIENT CALCULATION
CANCELLER COEFFICIENT CALCULATION
HILBERT TRANSFORM
CHANNEL MEASUREMENT
MATCHED FILTER CALCULATION
AUTOMATIC GAIN CONTROL
FROM RF RECEIVER

Fig. 4

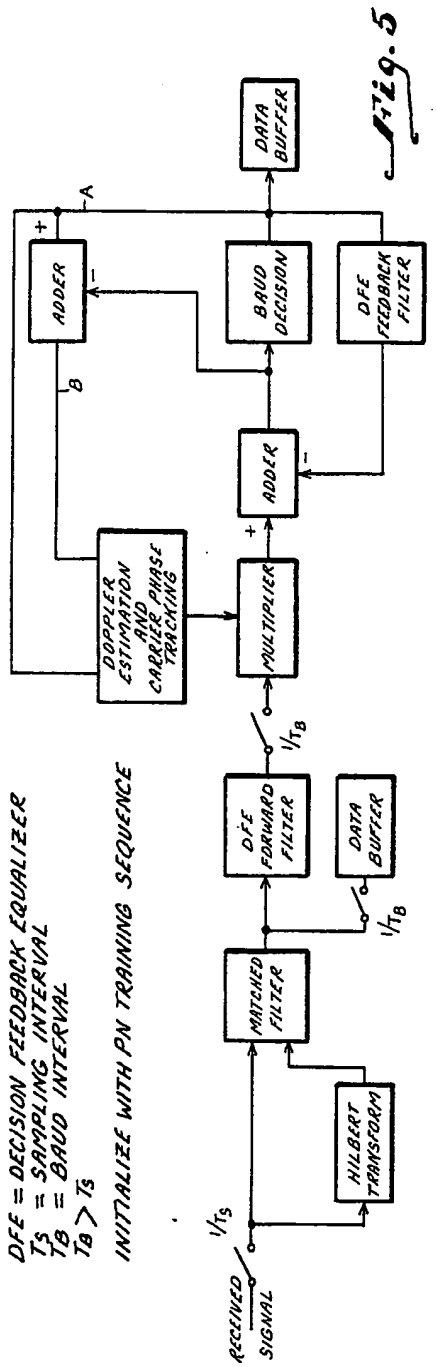

DFE = DECISION FEEDBACK EQUALIZER
T_S = SAMPLING INTERVAL
T_B = BAUD INTERVAL
$T_B > T_S$
INITIALIZE WITH PN TRAINING SEQUENCE
RECEIVED SIGNAL
$1/T_S$
HILBERT TRANSFORM
MATCHED FILTER
DFE FORWARD FILTER
DATA BUFFER
$1/T_B$
MULTIPLIER
DOPPLER ESTIMATION AND CARRIER PHASE TRACKING
ADDER
DFE FEEDBACK FILTER
BAUD DECISION
DATA BUFFER
A
B

Fig. 5

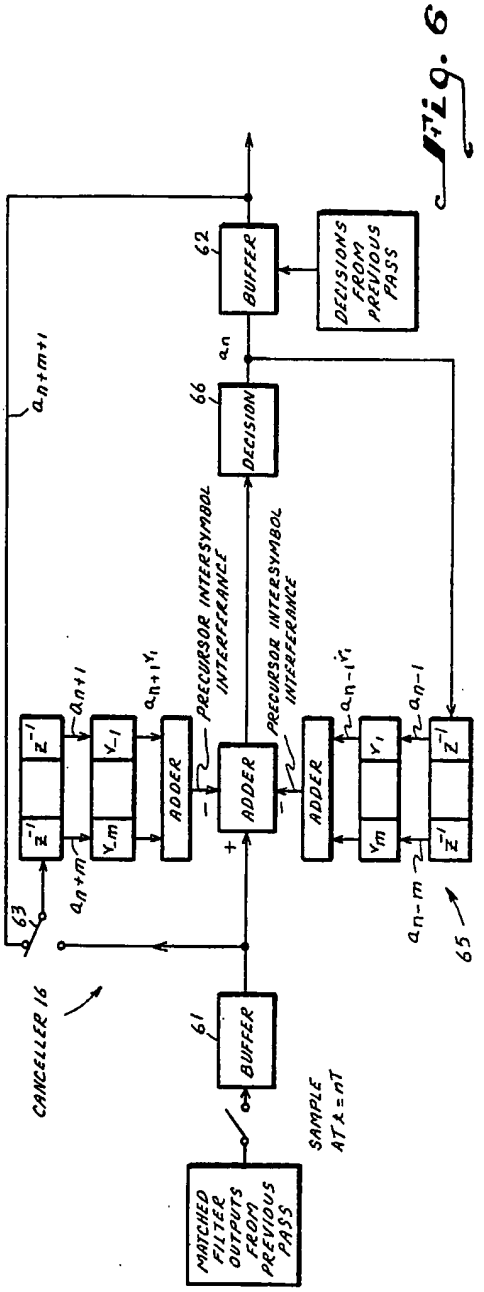

MATCHED FILTER OUTPUTS FROM PREVIOUS PASS
SAMPLE AT $t = nT$
BUFFER
CANCELLER 16
PRECURSOR INTERSYMBOL INTERFERANCE
ADDER
DECISION
BUFFER
DECISIONS FROM PREVIOUS PASS
a_{n+m+1}
a_{n+m}
a_{n+1}
a_{n-1}
a_{n-m}
Y_m
Y_1
Z^{-1}
61
62
63
65
66

Fig. 6

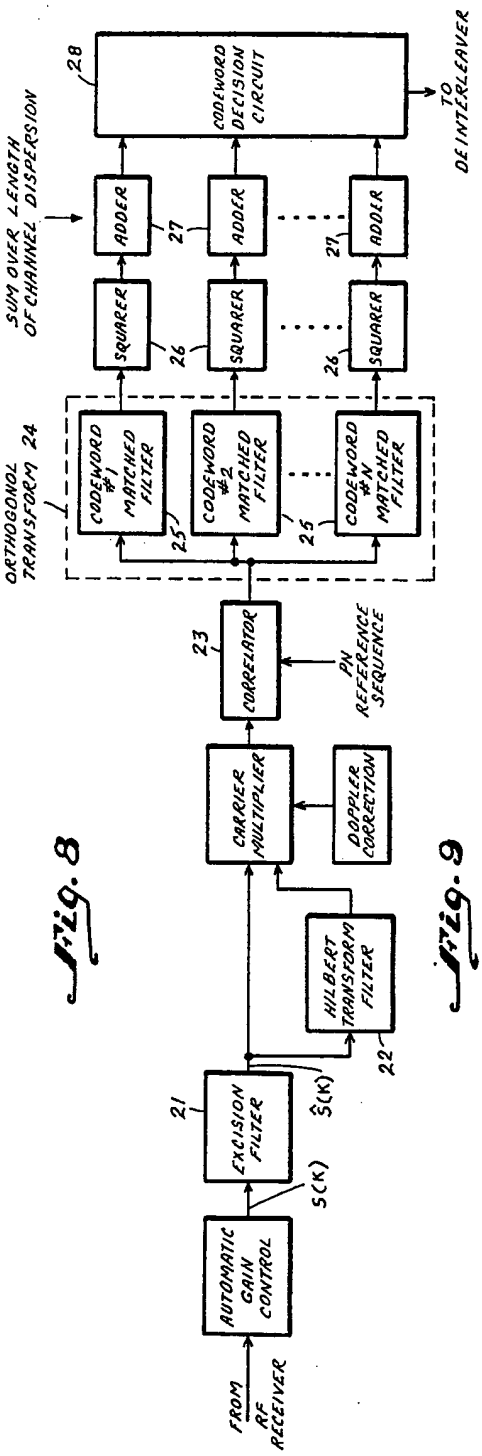

FROM RF RECEIVER
AUTOMATIC GAIN CONTROL
EXCISION FILTER
21
S(K)
Ŝ(K)
HILBERT TRANSFORM FILTER
22
CARRIER MULTIPLIER
DOPPLER CORRECTION
CORRELATOR
23
PN REFERENCE SEQUENCE
ORTHOGONOL TRANSFORM 24
CODEWORD #1 MATCHED FILTER
CODEWORD #2 MATCHED FILTER
CODEWORD #N MATCHED FILTER
25
SQUARER
26
ADDER
27
SUM OVER LENGTH OF CHANNEL DISPERSION
CODEWORD DECISION CIRCUIT
28
TO DEINTERLEAVER

Fig. 8

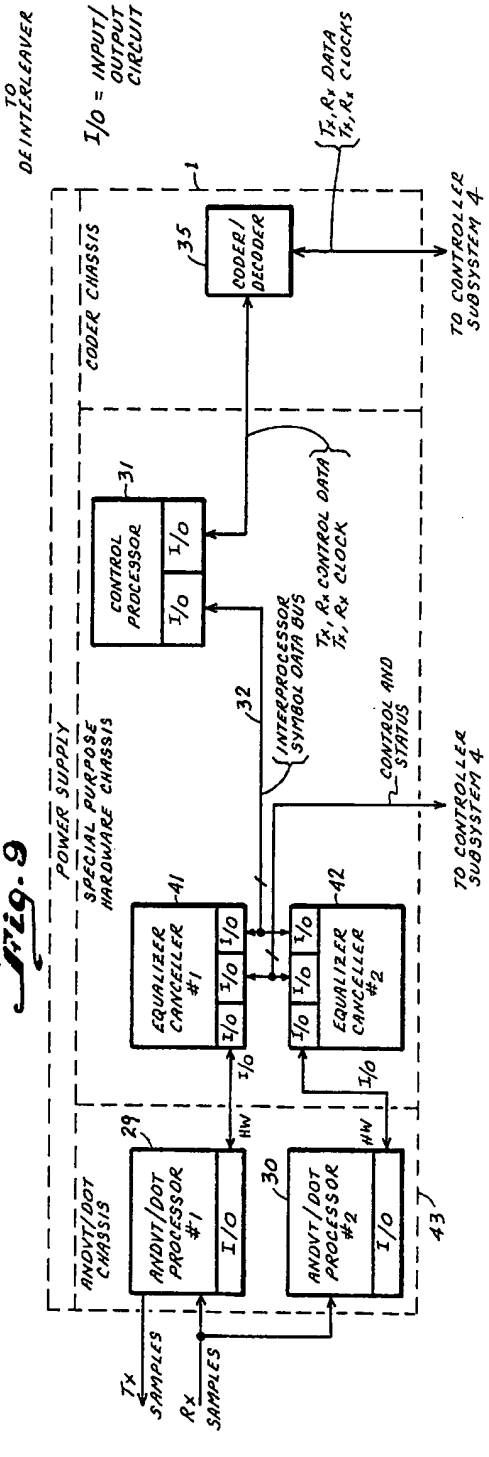
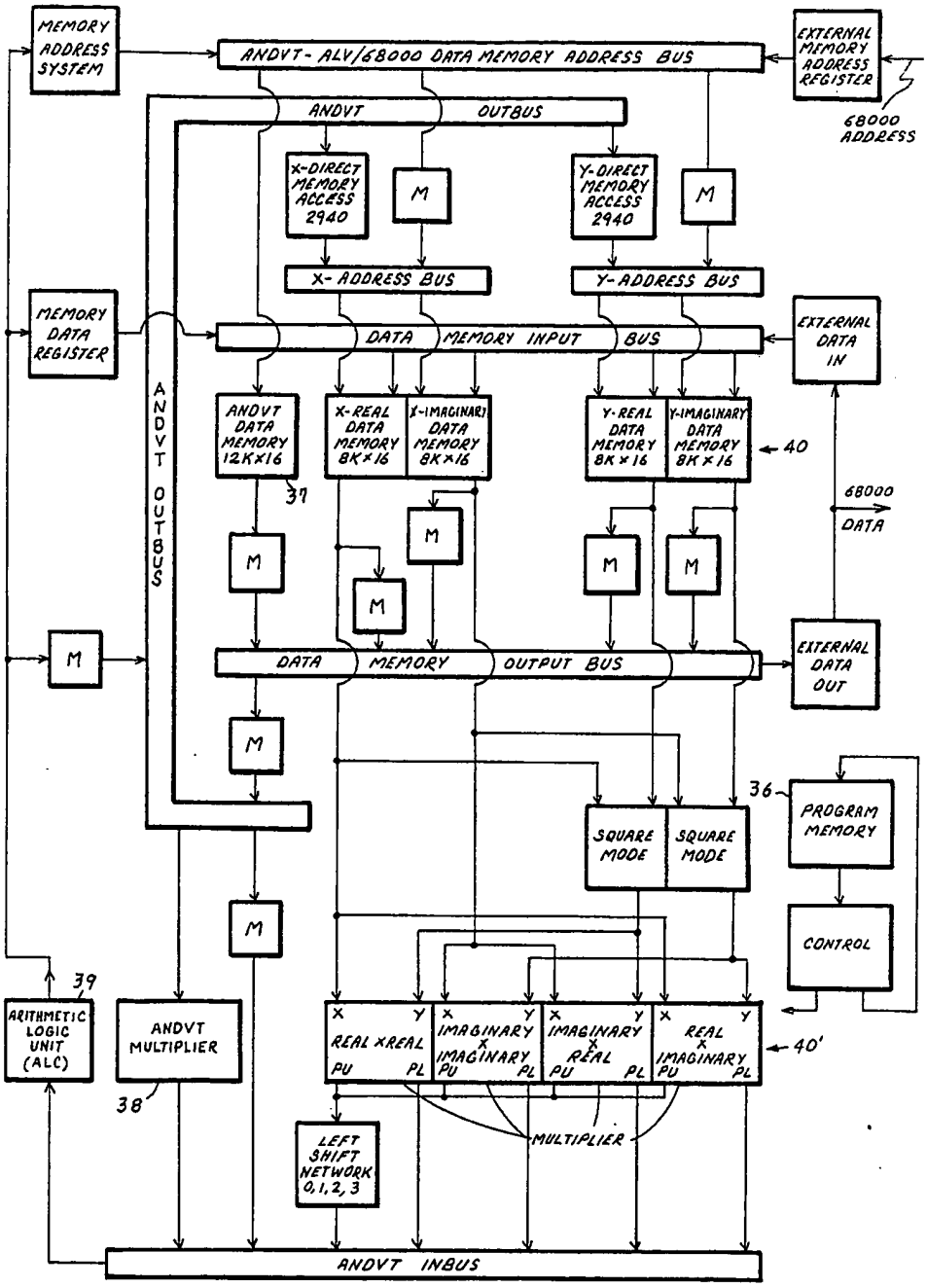

I/O = INPUT/ OUTPUT CIRCUIT
Tx, Rx DATA
Tx, Rx CLOCKS
CODER CHASSIS
CODER/ DECODER
35
TO CONTROLLER SUBSYSTEM 4
CONTROL PROCESSOR
31
I/O
Tx, Rx CONTROL DATA
Tx, Rx CLOCK
INTERPROCESSOR SYMBOL DATA BUS
32
CONTROL AND STATUS
TO CONTROLLER SUBSYSTEM 4
POWER SUPPLY
SPECIAL PURPOSE HARDWARE CHASSIS
EQUALIZER CANCELLER #1
41
EQUALIZER CANCELLER #2
42
HW
ANDVT/DOT CHASSIS
ANDVT/DOT PROCESSOR #1
29
ANDVT/DOT PROCESSOR #2
30
43
Tx SAMPLES
Rx SAMPLES

Fig. 9

Fig. 10



X and Y = COMPLEX NUMBERS
M = MULTIPLEXER

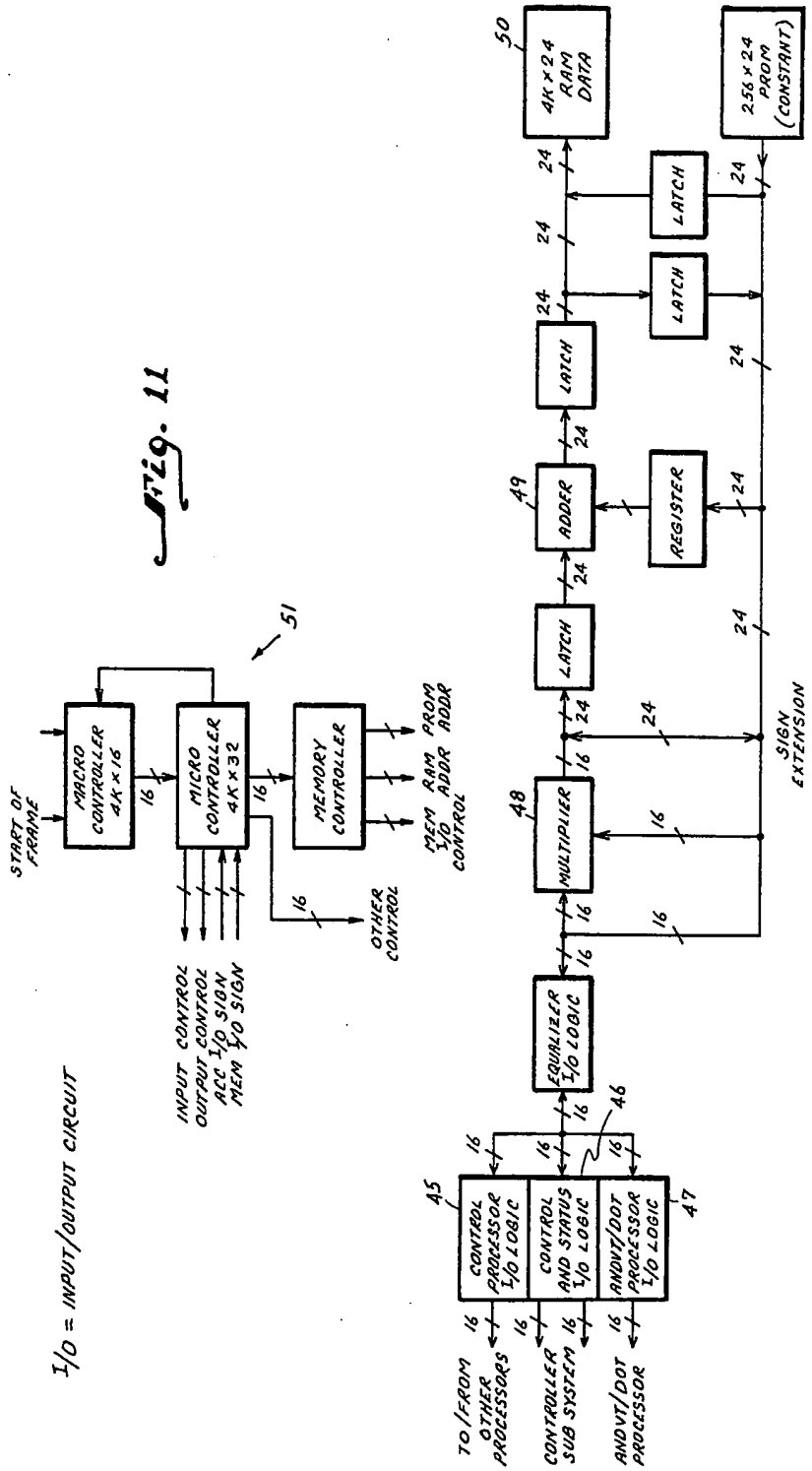

START OF FRAME
MACRO CONTROLLER 4K×16
MICRO CONTROLLER 4K×32
MEMORY CONTROLLER
PROM ADDR
RAM ADDR
MEM I/O CONTROL
OTHER CONTROL
INPUT CONTROL
OUTPUT CONTROL
ACC I/O SIGN
MEM I/O SIGN
51
4K×24 RAM DATA
256×24 PROM (CONSTANT)
LATCH
ADDER
REGISTER
MULTIPLIER
EQUALIZER I/O LOGIC
SIGN EXTENSION
CONTROL PROCESSOR I/O LOGIC
CONTROL AND STATUS I/O LOGIC
ANDVT/DOT PROCESSOR I/O LOGIC
TO/FROM OTHER PROCESSORS
CONTROLLER SUB SYSTEM
ANDVT/DOT PROCESSOR
I/O = INPUT/OUTPUT CIRCUIT

Fig. 11

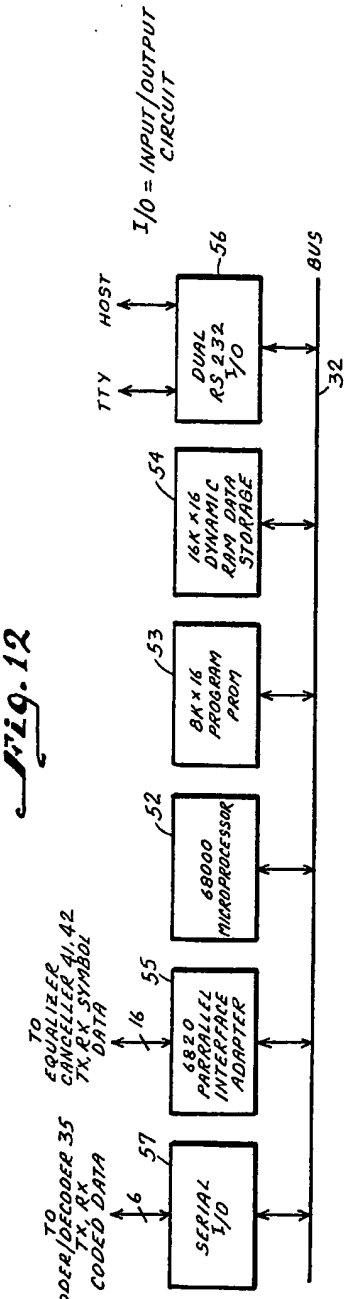


Fig. 12

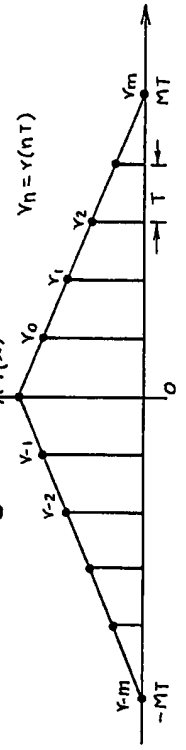


Fig. 14

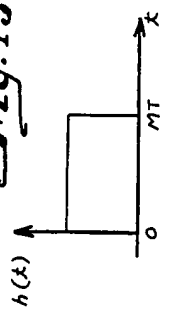


Fig. 13

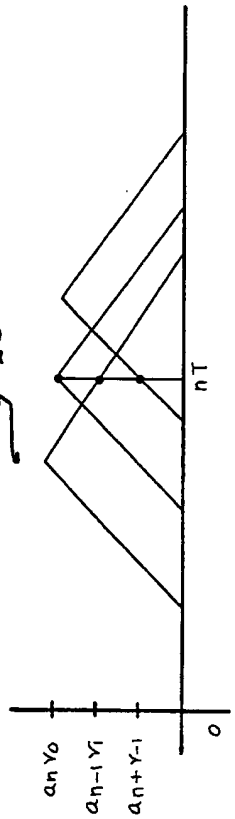


Fig. 15

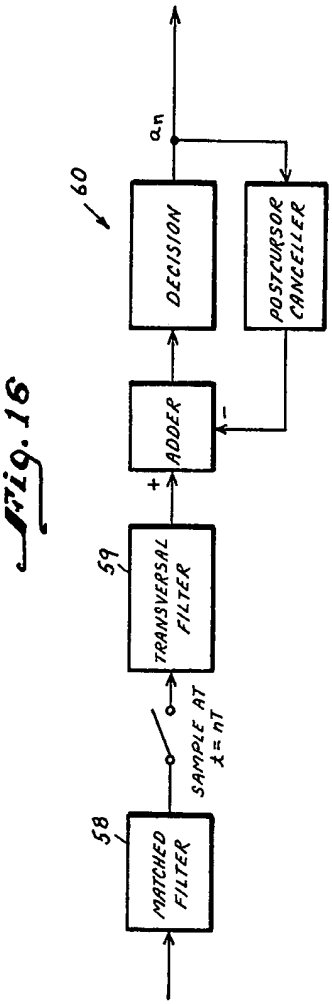

60
DECISION
POSTCURSOR CANCELLER
ADDER
TRANSVERSAL FILTER
SAMPLE AT $t = nT$
MATCHED FILTER
58
59
a_n

Fig. 16

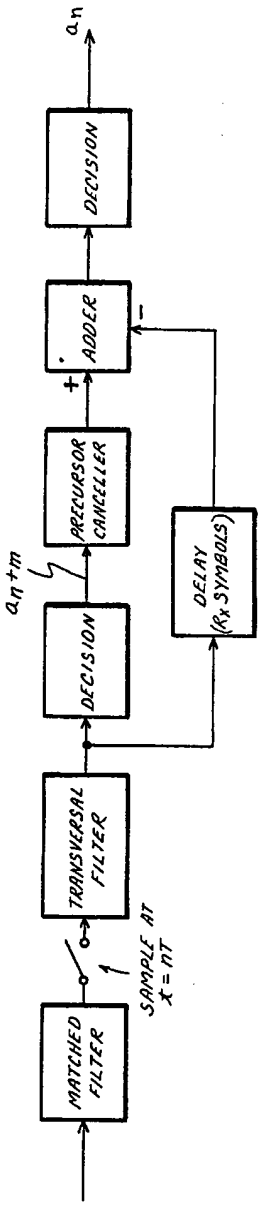

DECISION
ADDER
PRECURSOR CANCELLER
DELAY (K SYMBOLS)
DECISION
TRANSVERSAL FILTER
SAMPLE AT $t = nT$
MATCHED FILTER
a_{n+m}
a_n

Fig. 17

Fig. 18

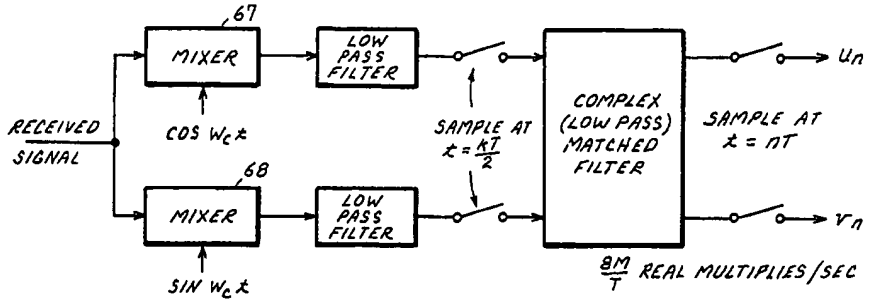


Fig. 19

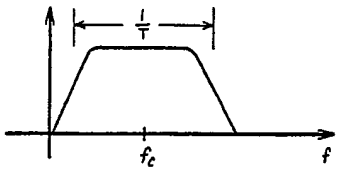


Fig. 20

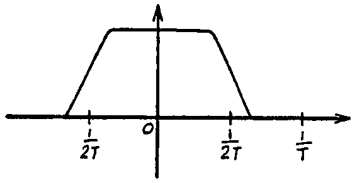


Fig. 21

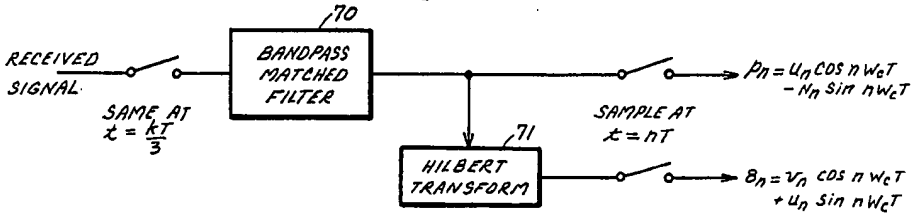
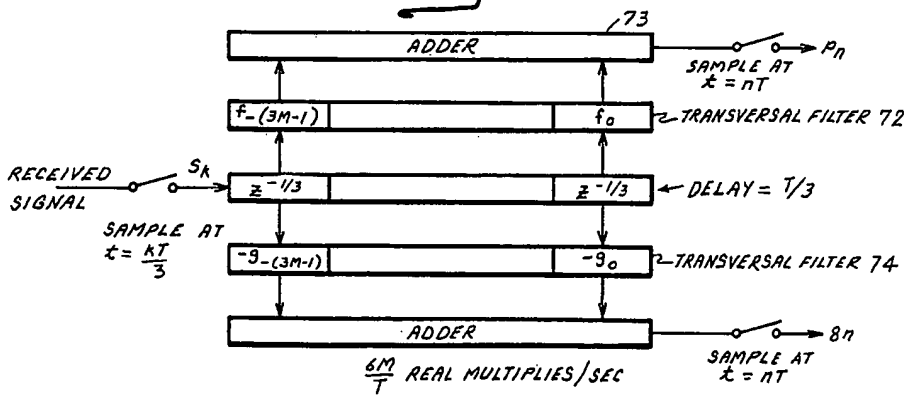


Fig. 22



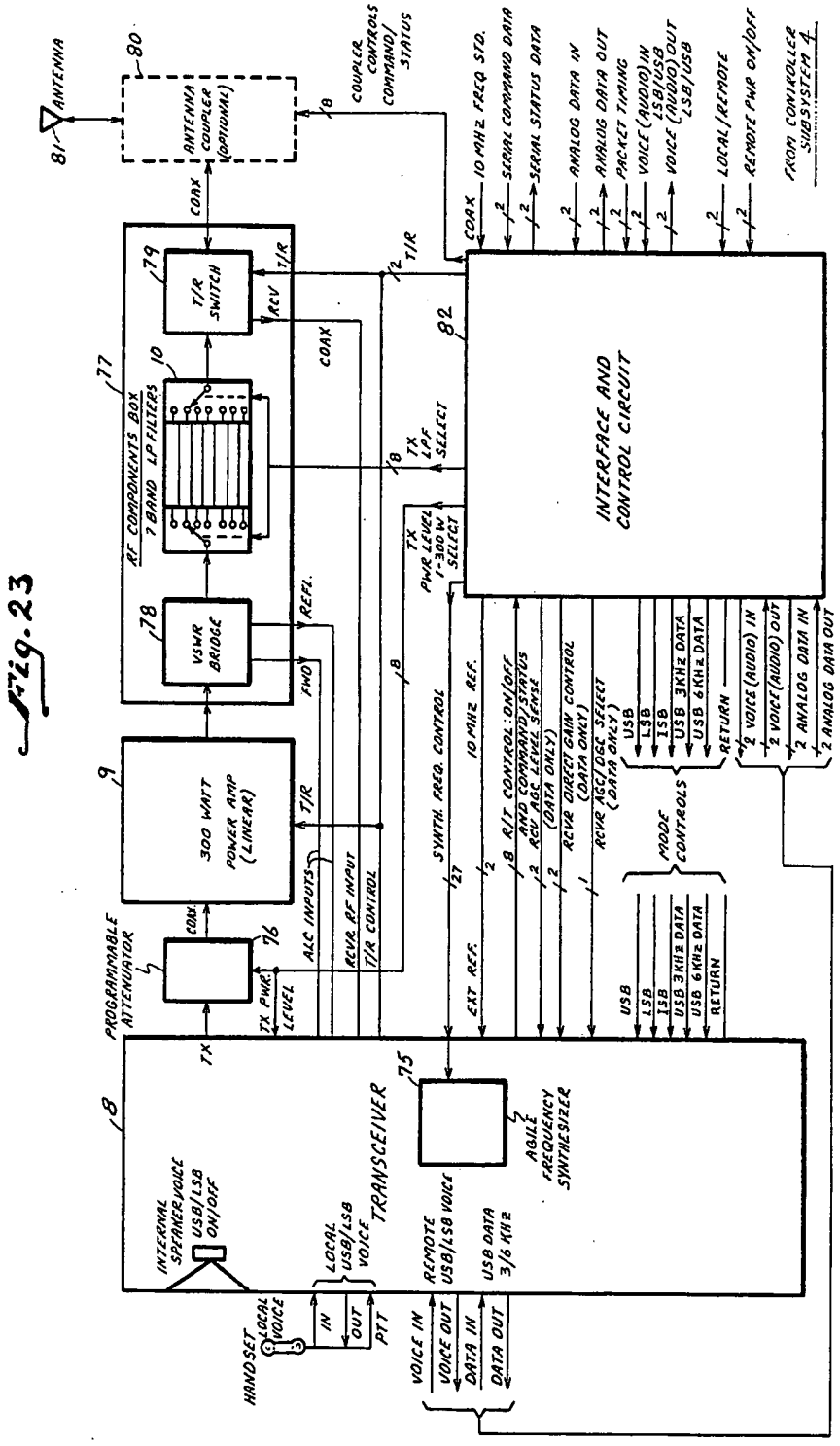

ANTENNA
81
80
ANTENNA COUPLER (OPTIONAL)
COUPLER CONTROLS COMMAND/ STATUS
COAX
79
T/R SWITCH
T/R
REV
77
RF COMPONENTS BOX
7 BAND LP FILTERS
10
COAX
82
INTERFACE AND CONTROL CIRCUIT
TX LPF SELECT
TX PWR LEVEL 1-300 W SELECT
78
VSWR BRIDGE
REFL
FWD
9
300 WATT POWER AMP (LINEAR)
T/R
PROGRAMMABLE ATTENUATOR
76
TX PWR LEVEL
ALC INPUTS
RCVR RF INPUT
T/R CONTROL
SYNTH. FREQ. CONTROL
10 MHz REF.
EXT REF.
8 R/T CONTROL: ON/OFF
AND COMMAND/STATUS
2 REV AGC LEVEL SENSE (DATA ONLY)
2 REVR DIRECT GAIN CONTROL (DATA ONLY)
1 REVR AGC/DSC SELECT (DATA ONLY)
MODE CONTROLS
USB
LSB
USB 3KHz DATA
USB 6KHz DATA
RETURN
2 VOICE (AUDIO) IN
2 VOICE (AUDIO) OUT
2 ANALOG DATA IN
2 ANALOG DATA OUT
10 MHz FREQ STD.
SERIAL COMMAND DATA
SERIAL STATUS DATA
ANALOG DATA IN
ANALOG DATA OUT
PACKET TIMING
VOICE (AUDIO) IN LSB/USB
VOICE (AUDIO) OUT LSB/USB
LOCAL/REMOTE
REMOTE PWR ON/OFF
FROM CONTROLLER SUBSYSTEM 4
8
TX
75
TRANSCEIVER
AGILE FREQUENCY SYNTHESIZER
INTERNAL SPEAKER/VOICE USB/LSB ON/OFF
LOCAL USB/LSB VOICE
REMOTE USB/LSB VOICE
USB DATA 3/6 KHz
HANDSET
LOCAL VOICE
IN
OUT
PTT
VOICE IN
VOICE OUT
DATA IN
DATA OUT

Fig. 23

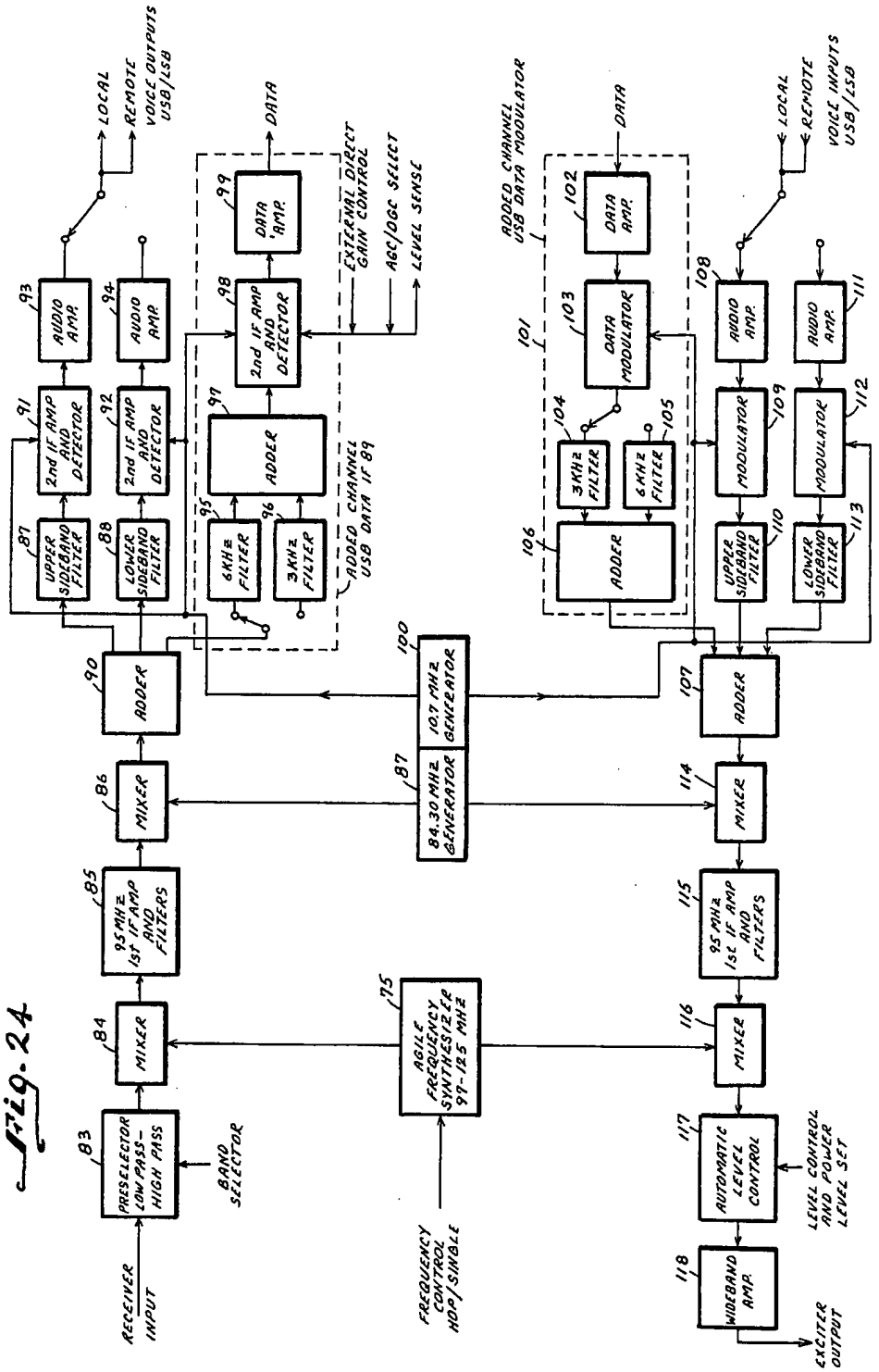

LOCAL
REMOTE
VOICE OUTPUTS USB/LSB
DATA
EXTERNAL DIRECT GAIN CONTROL
AGC/AGC SELECT
LEVEL SENSE
ADDED CHANNEL USB DATA MODULATOR
DATA
LOCAL
REMOTE
VOICE INPUTS USB/LSB
93 AUDIO AMP
94 AUDIO AMP
91 2nd IF AMP AND DETECTOR
92 2nd IF AMP AND DETECTOR
87 UPPER SIDEBAND FILTER
88 LOWER SIDEBAND FILTER
99 DATA AMP.
98 2nd IF AMP AND DETECTOR
97 ADDER
95 6KHz FILTER
96 3KHz FILTER
ADDED CHANNEL USB DATA IF 89
102 DATA AMP.
103 DATA MODULATOR
104 3KHz FILTER
105 6KHz FILTER
106 ADDER
101
108 AUDIO AMP.
111 AUDIO AMP.
109 MODULATOR
112 MODULATOR
110 UPPER SIDEBAND FILTER
113 LOWER SIDEBAND FILTER
90 ADDER
100 10.7 MHz GENERATOR
87 84.30 MHz GENERATOR
107 ADDER
86 MIXER
114 MIXER
85 95 MHz 1st IF AMP AND FILTERS
115 95 MHz 1st IF AMP AND FILTERS
84 MIXER
75 AGILE FREQUENCY SYNTHESIZER 99-125 MHz
116 MIXER
83 PRESELECTOR LOW PASS - HIGH PASS
BAND SELECTOR
117 AUTOMATIC LEVEL CONTROL
LEVEL CONTROL AND POWER LEVEL SET
118 WIDEBAND AMP.
RECEIVER INPUT
FREQUENCY CONTROL MOD/SINGLE
EXCITER OUTPUT

Fig. 24

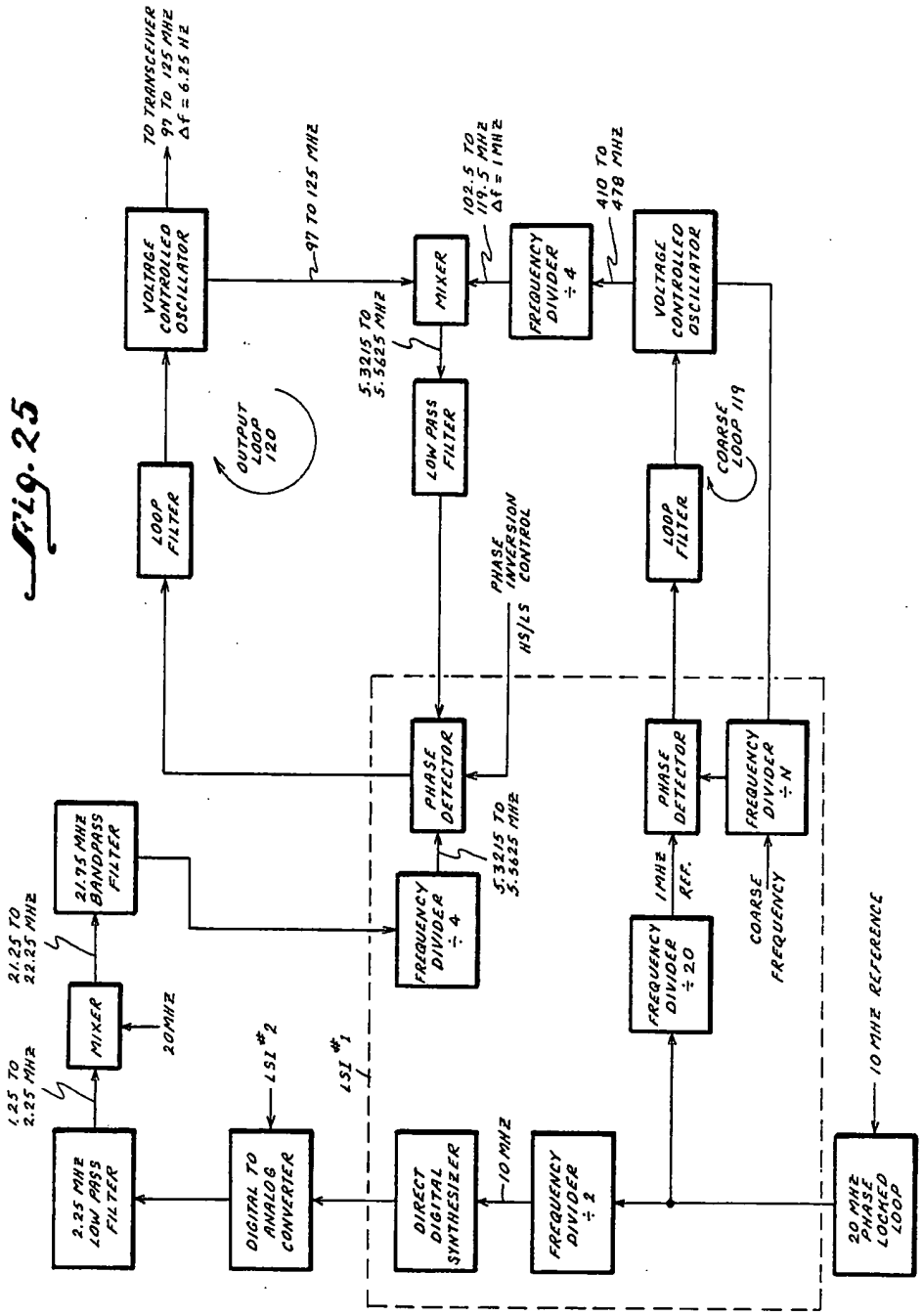

TO TRANSCEIVER
97 TO 125 MHz
Δf = 6.25 Hz
VOLTAGE CONTROLLED OSCILLATOR
97 TO 125 MHz
MIXER
102.5 TO 119.5 MHz
Δf = 1 MHz
FREQUENCY DIVIDER ÷ 4
410 TO 478 MHz
VOLTAGE CONTROLLED OSCILLATOR
5.3215 TO 5.5625 MHz
LOW PASS FILTER
OUTPUT LOOP 120
LOOP FILTER
PHASE INVERSION CONTROL
HS/LS
COARSE LOOP 119
LOOP FILTER
PHASE DETECTOR
PHASE DETECTOR
FREQUENCY DIVIDER ÷ N
21.75 MHz BANDPASS FILTER
5.3215 TO 5.5625 MHz
FREQUENCY DIVIDER ÷ 4
1 MHz REF.
FREQUENCY DIVIDER ÷ 20
COARSE FREQUENCY
21.25 TO 22.25 MHz
MIXER
20 MHz
1.25 TO 2.25 MHz
LSI #2
LSI #1
10 MHz REFERENCE
2.25 MHz LOW PASS FILTER
DIGITAL TO ANALOG CONVERTER
DIRECT DIGITAL SYNTHESIZER
10 MHz
FREQUENCY DIVIDER ÷ 2
20 MHz PHASE LOCKED LOOP

Fig. 25

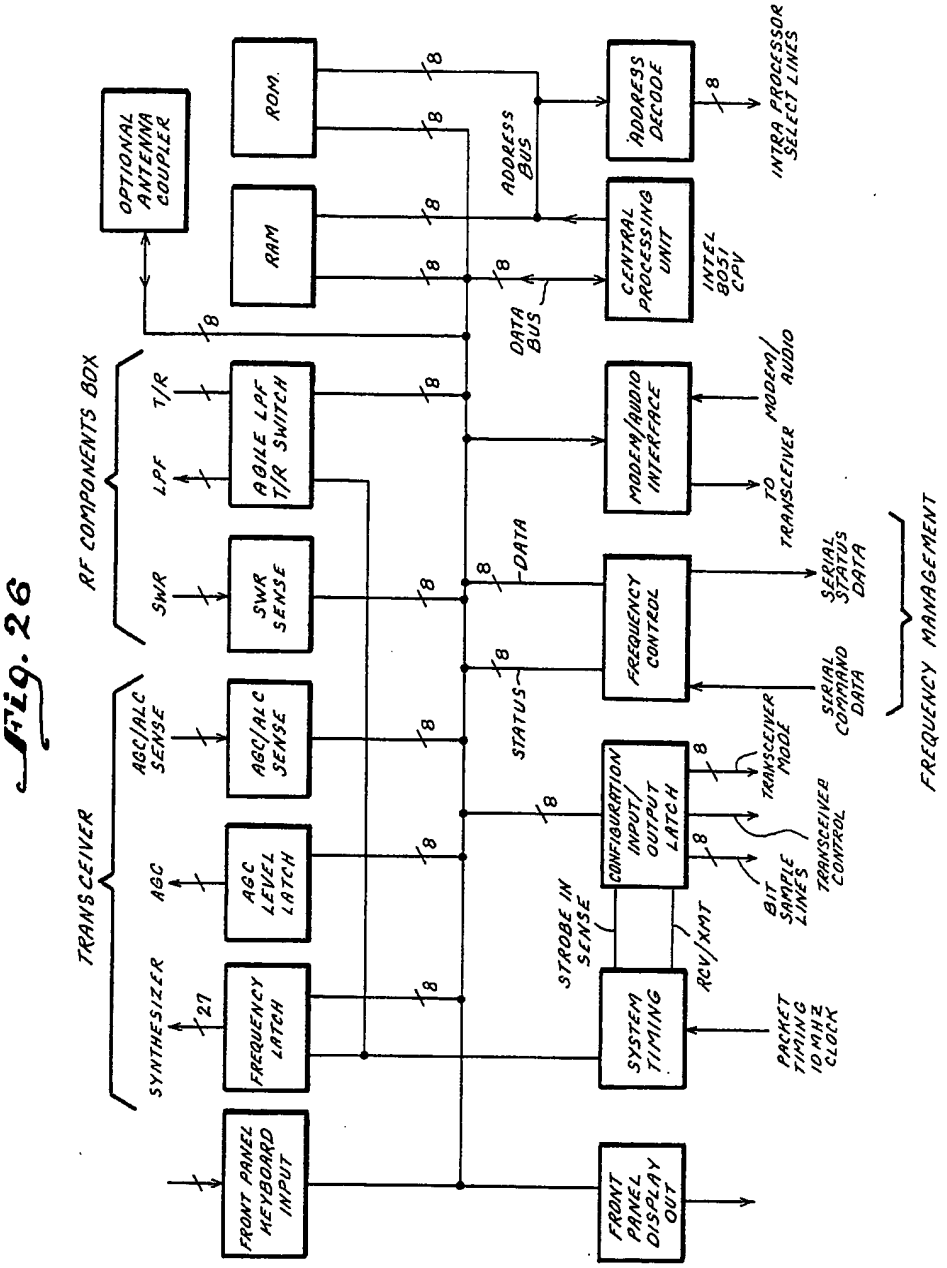

OPTIONAL ANTENNA COUPLER
ROM
RAM
ADDRESS BUS
ADDRESS DECODE
INTRA PROCESSOR SELECT LINES
CENTRAL PROCESSING UNIT
INTEL 8051 CPU
DATA BUS
RF COMPONENTS BOX
T/R
LPF
ABLE LPF T/R SWITCH
MODEM/AUDIO INTERFACE
MODEM/ AUDIO
TO TRANSCEIVER
SWR
SWR SENSE
DATA
FREQUENCY CONTROL
SERIAL STATUS DATA
TRANSCEIVER
AGC/ALC SENSE
AGC/ALC SENSE
STATUS
SERIAL COMMAND DATA
FREQUENCY MANAGEMENT
AGC
AGC LEVEL LATCH
CONFIGURATION INPUT/ OUTPUT LATCH
TRANSCEIVER MODE
SYNTHESIZER
21
FREQUENCY LATCH
STROBE IN SENSE
BIT SAMPLE LINES
TRANSCEIVER CONTROL
RCV/XMT
SYSTEM TIMING
PACKET TIMING 10 MHZ CLOCK
FRONT PANEL KEYBOARD INPUT
FRONT PANEL DISPLAY OUT

Fig. 26

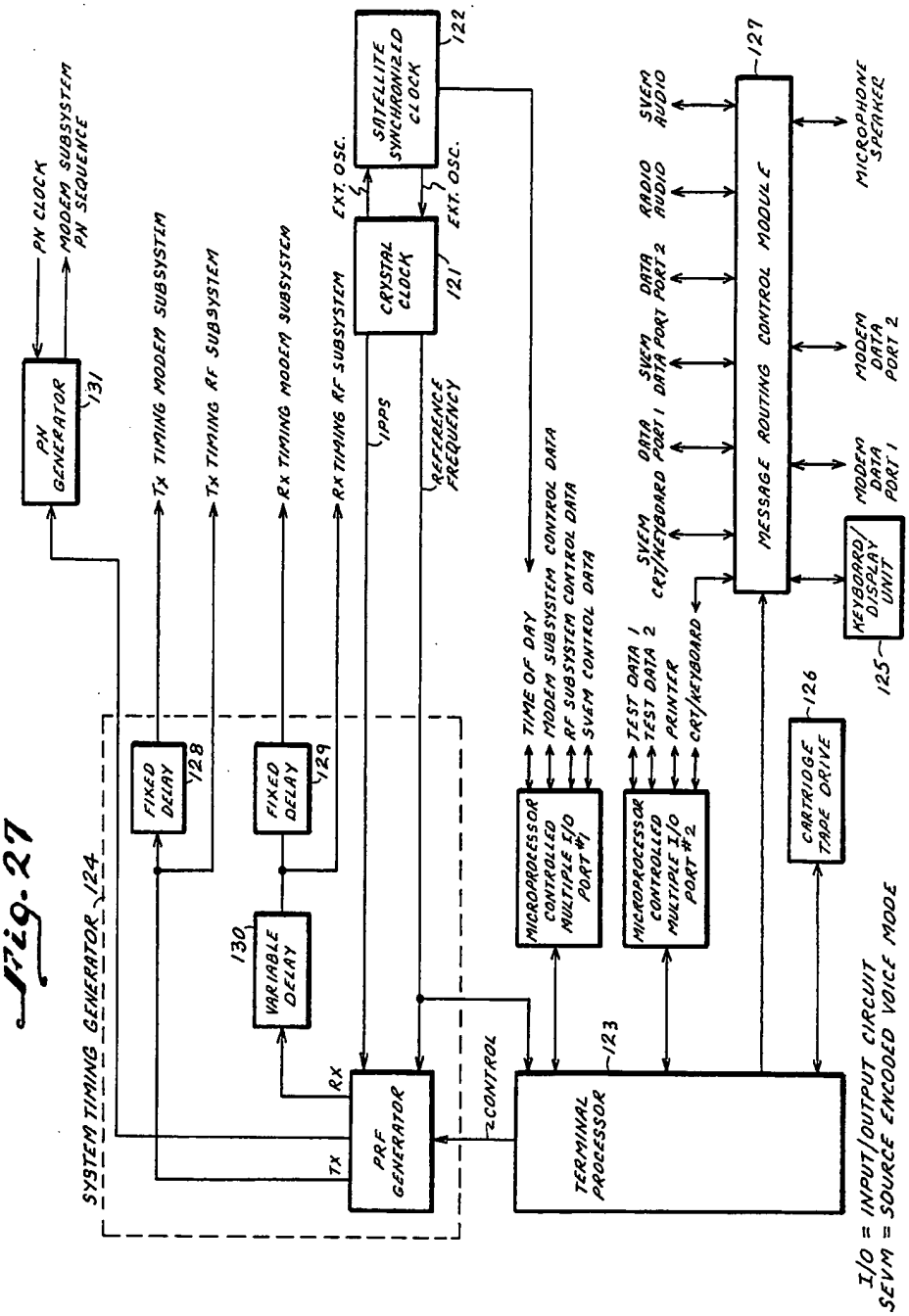

PN CLOCK
MODEM SUBSYSTEM PN SEQUENCE
PN GENERATOR
131
SATELLITE SYNCHRONIZED CLOCK
122
EXT. OSC.
CRYSTAL CLOCK
121
Tx TIMING MODEM SUBSYSTEM
Tx TIMING RF SUBSYSTEM
Rx TIMING MODEM SUBSYSTEM
Rx TIMING RF SUBSYSTEM
1PPS
REFERENCE FREQUENCY
TIME OF DAY
MODEM SUBSYSTEM CONTROL DATA
RF SUBSYSTEM CONTROL DATA
SVEM CONTROL DATA
SVEM AUDIO
RADIO AUDIO
DATA PORT 2
SVEM DATA PORT
DATA PORT 1
SVEM CRT/KEYBOARD
MESSAGE ROUTING CONTROL MODULE
127
MICROPHONE SPEAKER
MODEM DATA PORT 2
MODEM DATA PORT 1
KEYBOARD/ DISPLAY UNIT
125
FIXED DELAY
128
FIXED DELAY
129
VARIABLE DELAY
130
SYSTEM TIMING GENERATOR
124
MICROPROCESSOR CONTROLLED MULTIPLE I/O PORT #1
MICROPROCESSOR CONTROLLED MULTIPLE I/O PORT #2
TEST DATA 1
TEST DATA 2
PRINTER
CRT/KEYBOARD
CARTRIDGE TAPE DRIVE
126
RX
TX
PRF GENERATOR
CONTROL
TERMINAL PROCESSOR
123
I/O = INPUT/OUTPUT CIRCUIT
SEVM = SOURCE ENCODED VOICE MODE

Fig. 27

HIGH FREQUENCY SPREAD SPECTRUM COMMUNICATION SYSTEM TERMINAL

The Government has rights in this invention persuant to Contract No. F30602-83-C-0195 awarded by Rome Air Development Center, Department of the Air Force.

BACKGROUND OF THE INVENTION

The present invention relates to data communication systems and more particularly to a spread spectrum communication system terminal including sequence spreading and frequency hopping.

Spread spectrum communication systems have been used in a variety of fields. In the communication system of this type, the transmitted bandwidth is much greater than the bandwidth or rate of the information to be transmitted. The carrier signal is modulated by some other function to widen or spread the bandwidth for transmission. The received signal is remapped into the original information bandwidth to reproduce a desired signal. The spread spectrum communication system has many useful advantages: a selective call is possible; since the power spectrum density is low, private communication is allowed; and it is little influenced by interference either due to multipath fading or jamming. From this standpoint, the spread spectrum system has found many uses, such as mobile communication systems, avionic systems, satellite communications, scatter communication systems of both the ionospheric and tropospheric type, direction finders and distance measuring equipment.

The spread spectrum systems can be categorized into a direct sequence system, a frequency hopping system, a time hopping system and a hybrid system which is a proper combination of the systems just mentioned. Of these systems, the frequency hopping systems is frequently used in the field of mobile communication systems with a low traffic volume for a number of stations. Also frequency hopping systems can be employed in satellite communication systems and scatter type communication systems where a fading environment is present.

In the frequency hopping system a carrier frequency is shifted or jumped in discreet increments in a pattern dictated by a prepared code of sequence, for instance, a PN (psudo-noise), and M-sequence codes, Gold codes and the like, in synchronism with a change in the state of the codes. The resulting consecutive and time sequential frequency pattern is called a hopping pattern and the duration of each hopping frequency is called a chip. The transmitted information is embedded in the codes or embedded in each frequency of the carrier wave by a so-called FSK (frequency shift keyed) modulation. The information signal thus spread-spectrum-modulated can be reproduced at the receiver.

In reproducing the information signal at the receiver, a synchronization acquisition process is first performed, in which the code pattern provided in the receiver is made accurately coincident with the code pattern generated in the transmitter in time position. Then, the spread spectrum signal is despread, and thereafter a well known demodulation is performed to extract the desired information. More particularly, a local reference signal of a frequency correspondingly determined by the same code pattern as that in the transmitter for every chip and the received signal are mixed in a mixer in order to perform a correlation (despreading) process for converting the spread spectrum signal into the signal having a frequency bandwidth wide enough to extract the information. This system is described in detail in "Spread Spectrum Systems" by R. C. Dixon published by John Wiley and Sons, Inc. in 1976. Following this despreading process, the desired information is extracted by usual demodulation techniques.

It is also known to employ a direct sequence system again employing a PN code, M-sequence codes, Gold codes and the like to spread the transmitted information over the bandwidth of the system and to again employ correlation technique at the receiver to recover the information.

Such systems are not only useful in obtaining a proper coherent transmission in a fading environment, such as is present in mobile communication, satellite communications and scatter communication, the systems are also jammer resistant.

High frequency radio data communication systems have gained increasing importance in recent years where it is used for long distance radio contact as a backup or adjunct to satellite networks. As the high frequency band (2–30 megahertz (MHZ)) is more widely used, the need for reliable high frequency communication links increases. To improve the performance of data modems in terms of bit error rates, recovery from fade dropouts, intersymbol interface due to multipath dispersion effects, and immunity to interference state of the art equalization and error correction techniques must be applied. In addition, spread spectrum signal processing techniques are required to provide antijam capability and low probability of intercept capability.

SUMMARY OF THE INVENTION

An object of the invention is to provide an improved high frequency radio data communication system.

Another object of the present invention is to provide a high frequency radio data communication system terminal employing an improved modem subsystem which improves the performance in terms of bit error rate, recovery from fade dropouts, intersymbol interface due to multipath dispersion effects, and immunity to inteference employing equalization and error correcting techniques in addition to spread spectrum signal processing techniques.

Still another object of the present invention is to provide a high frequency spread spectrum communication terminal having improved performance in terms of bit error rate, recovery from fade dropouts, intersymbol interface due to multipath dispersion effects, and immunity to inteference employing equalization and error correcting techniques in addition to spread spectrum signal processing techniques to provide antijam capability and low probability of intercept.

A feature of the present invention is the provision of a spread spectrum communication system terminal comprising: a first subsystem including first means to encode locally generated digital data with an error correcting code, second means coupled to the first means for spectrum speading of the encoded locally generated digital data in at least one mode of operation of the communication system terminal, third means to receive remotely generated error correcting code encoded digital data spectrum spread in the one mode of operation, and fourth means coupled to the third means to recover the remotely generated digital data; a second subsystem including fifth means frequency hopping the

encoded locally generated digital data prior to transmission to a remote location, and sixth means frequency dehopping the encoded remotely generated digital data received from the remote location; and a third subsystem including seventh means coupled to the second means and the fifth means to provide a predetermined signal for spectrum spreading of the encoded locally generated digital data in the one mode of operation and to couple the encoded locally generated digital data to the fifth means, and eighth means coupled to the third means, the fifth means and the sixth means to provide a reference frequency for the frequency hopping and the frequency dehopping and to couple the frequency dehopped encoded remotely generated digital data from the sixth means to the third means.

Another feature of the present invention is the provision of providing in a communication system employing frequency hopping and spread spectrum techniques, a modem subsystem comprising: first means to encode locally generated digital data with an error correcting code, second means coupled to the first means for spectrum spreading of the encoded locally generated digital data in at least one mode of operation of the communication systems and to couple resultant digital data to a radio frequency subsystem for frequency hopping, third means coupled to the radio frequency subsystem to receive remotely generated error correcting code encoded digital data spectrum spread in the one mode of operation and frequency dehopped in the radio frequency subsystem, and fourth means coupled to the third means to recover the remotely generated digital data.

BRIEF DESCRIPTION OF THE DRAWING

The above-mentioned and other objects and features of the present invention and the manner of obtaining them will become more apparent by reference to the following description taken in conjunction with the drawing, in which

FIG. **1** is a basic block diagram of the spread spectrum communication system terminal in accordance with the principals of the present invention;

FIG. **2** illustrates the packet transmission format for each of the two modes of operation of the communication system terminal of FIG. **1**;

FIG. **3** is a block diagram illustrating the algorithm for the high data rate (HDR) transmission function of the terminal of FIG. **1**;

FIG. **4** is a block diagram illustrating the algorithm for the HDR mode for the receiving operation of the terminal of FIG. **1**;

FIG. **5** is a block diagram illustrating the algorithm for the first pass in the decision feedback equalizer for the HDR mode of operation of the terminal of FIG. **1**;

FIG. **6** is a block diagram illustrating the algorithm of the second and third pass for the equalizer canceller in the HDR mode of operation of the terminal of FIG. **1**;

FIG. **7** is a block diagram illustrating the algorithm for the transmission function of the terminal of FIG. **1** in the JR (jam resistant) mode of operation thereof;

FIG. **8** is a block diagram illustrating the algorithm of the receiving function of the terminal of FIG. **1** in the JR mode of operation thereof;

FIG. **9** is a lot more detailed block diagram of the modem subsystem of FIG. **1**;

FIG. **10** is a general block diagram of the ANDVT/-DOT processors of FIG. **9**;

FIG. **11** is a block diagram of the equalizer canceller of FIG. **9**;

FIG. **12** is a block diagram of the control processor of FIG. **9**;

FIG. **13** is a waveform illustrating the overall impulse response of the transmit filter and channel;

FIG. **14** is a waveform illustrating the overall impulse response of the transmit filter, channel and matched filter of the terminal of FIG. **1**;

FIG. **15** is a waveform illustrating intersymbol interference;

FIG. **16** is a block diagram illustrating the algorithm of the decision feedback equalizer of FIG. **9**;

FIG. **17** is a block diagram illustrating the algorithm of the decision feedforward equalizer that could be substituted for the feedback equalizer of FIG. **16**;

FIG. **18** is a block diagram illustratng the quadrature demodulation approach for a bandpass matched filter;

FIG. **19** is a waveform illustrating the received signal bandpass spectrum;

FIG. **20** is a waveform illustrating the received signal low pass spectrum;

FIG. **21** is a block diagram illuatrating the algorithm for a bandpass filtering approach for a matched filter;

FIG. **22** is a block diagram illustrating a matched filter implementation;

FIG. **23** is a more detailed block diagram of the RF subsystem of the terminal of FIG. **1**;

FIG. **24** is a block diagram of the tranceiver of FIGS. **1** and **23**;

FIG. **25** is a block diagram of the agile frequency synthecizer of FIGS. **1**, **23** and **24**;

FIG. **26** is a block diagram illustrating the RF interface and control circuit of FIGS. **1** and **23**;

FIG. **27** is a block diagram of the controler subsystem of FIG. **1**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Refering to FIG. **1**, there is illustrated therein a general block diagram of a terminal for a high frequency spread spectrum communication system in accordance with the principals of the present invention. The terminal includes a modem subsystem **1** which uses state of the art equalization techniques and spread spectrum signal processing. The terminal of the communications system provides for 4800 bits per second and 2400 bits per second data communication on 6 kHz (kilohertz) and 3 kHz high frequency channels with frequency hopping by the radio frequency (RF) transmitter/-receiver which is contained in the RF subsystem **2**. Frequency hopping combined with decision feedback equalization, linear intersymbol interference cancellation, error correction and interleaving in the model subsystem **1** gives frequency diversity and antijam capability. Very low bit rate voice communication via voice recognition in voice subsystem **3** is also provided by the high frequency communication system terminal. In this mode of operation the modem subsystem **1** uses PN spreading to utilize the full bandwidth that is available and provide additional antijam capability. The frequency hopping/PN technique also gives low probability of intercept capability if low transmission powers are used.

The high frequency communication system provides the following capabilities:

(1) 2400 bits/second and 1200 bits/second data communication in a 3 kHz bandwidth high frequency channel,

(2) 4800 bits/second data communication in a 6 kHz bandwidth high frequency channel,

(3) low bit rate data communication with PN spreading to the specified channel bandwidth,

(4) frequency hopping operation during communication at all of the above data rates and channel bandwidths and,

(5) voice recognition of discrete utterances from a fixed vocabulary to enable low bit rate voice communication.

The communication terminal shown in FIG. 1 of the communication system includes a controller subsystem 4 in addition to modem subsystem 1, RF subsystem 2 and voice subsystem 3. Each subsystem performs as a stand alone function witn a well defined flexible interface. This allows for the possibility of taking a given subsystem and using it to perform a similar function in a different communication system. The controller subsystem 4 provides overall centralized control of the terminal and monitors the other subsystems through control/status lines. Controller 4 performs the tasks of system initialization, mode set up, interconnection between peripherial devices in different subsystem, performance testing and data recording. Packet timing is generated in controller 4 through the use of a crystal clock with an accuracy of 2×10^{-10}. This timing is synchronized to the NOAA "GOES" satellite and compensated for signal propagation delay. Additional tasks for controller 4 are the generation of a PN stream and the control of the RF frequency hopping operation.

Low bit rate digital speech is generated by voice subsystem 3 by voice recognition. Voice subsystem 3 accepts speech input from a microphone and produces digital data code words from a fixed vocabulary which corresponds to the recognized utterances in speech recognition circuit 5 and mass memory 6. On the receive side, voice subsystem 3 accepts digital data and synthesizes audio signals corresponding to the transmitted utterances in speech synthesizer 7 and mass memory 6. Voice subsystem 3 is trained by the speaker on a vocabulary of 255 utterances. Templates for up to four speakers can be stored in memory 6. The recognition accuracy is 96% in a laboratory environment. Subsystem 3 uses an Intel bubble memory with four million bits per cartridge for mass storage, 68000 microprocessors for recognition in circuit 5 and a TMS 32010 processor in synthesizer 7 for digital filtering of the audio signals.

Modem subsystem 1 accepts digital data at rates up to 4800 bits/second. This data is encoded with an error correcting code interleaved to minimize the effects of burst errors, grouped into packets, encoded into an eight phase complex symbol digital filtered at baseband and modulated on to a carrier, sent to an analog to digital converter and output to RF subsystem 2. On the received side, modem subsystem 1 removes narrowband inteferrence and compensates for the time dispersion and fading of the high frequency medium as well as reversing the action of the transmitter. Details of modem subsystem 1 will be described hereinbelow.

RF subsystem 2 provides a frequency hopping high frequency amplifier of transceiver 8 for data communication as well as normal single sideband (SSB) voice operation in the 2-30 MHZ band. The SSB voice operation is USB (upper side band), LSB (lower side band), or ISB (intermediate side band). The receiver of transceiver 8 has a dynamic range from −110 dBM (decibel) to −10 dBM with a 10 dBS signal to noise ratio at −110 dBM. Automatic gain control for transceiver 8 can be operated automatically or by external selection. Data modes provide 3 or six kHz bandwidths. Frequency hopping steps are 6.25 hz (hertz) increments with a settling time of 1 milliseconds (ms). The power amplifier 9 provides 300 watts with an angle low pass filter and power detector 10 to surpress harmonics.

The signal processing in modem subsystem 1 can be described by two different sets of algorithms. The high data rate (HDR) algorithms are used when the data rates are 4800 bits/seconds, 2400 bits/seconds or 1200 bits/seconds. The jam resistant (JR) algorithms are used when the input data rates are low and PN spreading is performed to provide spread spectrum advantage. Frequency hopping is used in both the HDR and JR modes of operation. Modem subsystem 1 processes data in blocks which are called packets. The packet formats for the two modes of operation are shown in FIG. 2. Packet lengths are fixed and all of the data from any single packet are transmitted at a single frequency.

FIG. 3 shows the algorithm for the transmitter function for the HDR mode. The data bits are scrambled in scrambler 11 to insure randomness over a packet interval, then they are passed through a error correction encoder 12 which is followed by an interleaving algorithm in interleaver 13. Next, PSK (phase shift key) modulation is performed in encoder 14 and the modulated signal is filtered in transmit shaping filter 15. The filter characteristics of filter 15 are chosen to limit the peak to RMS (root mean square) power ratio of the transmitted signal to less than 2 dB and to restrict the bandwidth of the transmitted signal. The filter impulse response is given by the expression:

$$h(k)=\sin(pi\ k\ b)/(pi\ k\ b)\cos(pi\ a\ k\ b)/(1.-(2\ a\ k\ b)^2) \quad (1)$$

where,

k is the sample index

a is a constant between 0 and 1

b is a constant related to the product of the sampling interval and the filter 3 dB bandwidth

At the beginning of each packet a training sequence is transmitted. This sequence is used by the demodulator to calculate the HF channel impulse response. The algorithm for the receiving functon in the HDR mode is shown in FIG. 4. A non-iterative form of equalization is used to compensate for the mutipath effects of the HF propagation channel. The equalization and demodulation are perfomed in a two pass process on each packet of data. First, the training sequence is used to calculate the coefficients for a decision feedback equalizer (DFE) and a matched filter. The received data samples are passed through the DFE and a set of decisions for an entire packet of data is stored. Next, a set of coefficients for a linear canceller is calculated and the received data samples are passed through the canceller and the set of DFE decisions is used to cancel intersymbol interference. The operations performed on the first pass are diagrammed in FIG. 5. In the first operation the training sequence is used to estimate the high frequency channel impulse response. The training sequence is a complex PN sequence of length N with a cyclic autocorrelation function given by:

$$R(k-m) = N \text{ for } k=m \quad (2)$$
$$= O \text{ for } k <> m$$

Two period of the training sequence are transmitted. The received signal samples are correlated with a modulated replica of the training sequence. The result of this correlation is an estimate of the channel impulse response. The channel impulse response estimate is given by:

$$h(k)=\text{SUM}_{n=0}^{N}[s(k+n)pt(n)] \quad (3)$$

where,

s(n)=nth complex sample of received signal

pt(n)=nth complex sample of training sequence

N=length of training sequence

Using the coefficients h(k), tap weights for a matched filter and a DFE can be calculated. The matched filter coefficients are

$$f(k)=h^*(JM-k) \quad (4)$$

where,

M=length of the channel impulse response in symbols,

J=ratio of sample rate to symbol rate, and

h*(n)=complex conjugate of h(n).

The optimum DFE forward filter coefficients can be computed by solving the set of linear equations for u(n) as given by Mueller and Salz, "A Unified Theory of Data-Aided Equalization," Bell System Technical Journal, Vol. 60, No. 9, pp. 2023–2039, November 1981:

$$\text{SUM}_{n=0}^{m}[u(n)\,X(k-n)] = X(k) \text{ for } k=0,1\ldots,M \quad (5)$$

where, (6)

$u(n)$ = *nth DFE* forward filter parameter,

$$X(m)=\text{SUM}_{n=0}^{JM}[h(n)h^*(JM+n)] \text{ for } m=1,\ldots,M,$$

$$X(0)=\text{SUM}_{n=0}^{JM}[h(n)h^*(n)] + NP, \quad (7)$$

j = ratio of sampling rate to symbol rate, and

NP = received noise power.

The DFE forward filter coefficients, c(n), are given by the equations:

$$c(0)=(1-u(0))/NP, \text{ and}$$

$$c(n)=-u(n)/NP \text{ for } n=1,\ldots,M.$$

The set of linear equations in (5) can be solved directly for c(n) by making a change of variable to give:

$$\text{SUM}_{n=0}^{M}[c(n)x(k-n)] = Y(k) \text{ for } k=0,1,\ldots,M \quad (7a)$$

where

-continued

$$Y(0) = 1.0, \text{ and} \quad (7b)$$
$$Y(k) = 0.0 \text{ for } k=1,2,\ldots,M.$$

This is a hermetian set of linear Toeplitz equations which can be solved efficiently using Zohar's algorithm as found in "The Solution of a Toeplitz Set of Linear Equations," Journal of the Association for Computing Machinery, Vol. 21, No. 2, pp. 272–276, April 1974.

The coefficients for the DFE feedback filter are given by

$$b(n)=\text{SUM}_{m=0}^{M}[c(m)w(M+n-m)] \text{ for } n=1,2,\ldots,M \quad (8)$$

where

$$w(m)=\text{SUM}_{k=0}^{JM}[h(k)f(Jm-k)] \text{ for } m=0,1,\ldots,2M \quad (9)$$

The operations in the second processing pass are shown in FIG. 6. The received data samples are passed through a matched filter and a linear canceller. The tap weights for the linear canceller **16** are given by the expression for w(m) in equation (9) above.

The algorithm and functional data flow for the modem subsystem **1** operating in the JR mode is shown in FIG. 7. In this mode of operation the input data rate is very low and there are a small number of data bits per packet. These data bits are encoded into a group of orthogonal codecwords by orthogonal encoder **17** and the code words are used to phase modulate a PN sequence by means of PSK baud encoder **18** and modulator **19**. The data from a data device is as in the HDR mode scrambeled in scrambeler **11**, error correcting encoded in encoder **12** and subjected to an interleaving algorithm in interleaver **13**. The modulated PN sequence is filtered in transmit shaping filter **20** and then transmitted. The functional flow and algorithm for the receiver functions in the JR mode of operation is shown in FIG. **8**. A narrowband jammer excision filter **21** of the type described by J. W. Ketchum and J. G. Proakis "Adaptive Algorithms for Estimating and Suppressing Narrow-Band Inteference in PN Spread Spectrum Systems", IEEE Transactions on Communications, Vol., COM-30, No 5, pp. 913–924, May 1982 is used to widen the signal and compensate for the effects of tone jammers. Excision filter **21** is an M+1 tap filter with coefficients,

a(m); m=0,1,...,M

The coefficients, a(m), are obtained by solving a set of M linear equations given by

$$\text{SUM}_{m=1}^{M}[a(m) * rho(k-m)] = rho(k);\ k=1,2,\ldots,M \quad (10)$$

where

$$rho(k) = \quad (11)$$

$$\text{SUM}_{n=0}^{NSAMP/J-j*M}[s(j*n)*s(j*(n+k))];\ k=0,1,\ldots,M$$

-continued

$a(0) = -1.0$

j = ratio of sample rate to PN chip rate

$NSAMP$ = number of samples in a received packet

The equations are solved for a(1) to a(M). The received signal is then filtered to give

$$s(k) = -\sum_{m=0}^{M} [a(m) * s(k-m)] \quad (12)$$

Following excision filter **21** a non-coherent detection scheme is used to select the othogonal code word which produces the largest correlation response energy. The output of filter **21** is passed through a Hilbert transform filter **22** to generate a complex signal. This signal is correlated with PN reference sequence in correlator **23**. Correlator **23** is followed by an orthogonal transform **24** which is equivalent to passing the signal through filters matched to each of the possible orthogonal code words. The outputs of the matched filters **25** are passed through squares **26** and adders **27**. The code word for the largest output is chosen as the received data by code word decision circuit **28**.

The hardware of modem subsystem **1** shown in greater detail in FIG. **9** and is designed to handle the computational load and the system interfaces by means of specialized blocks. The computational loads of modulation and demodulation are handled by three processors. The high speed signal processing calculations are performed by two processors **29** and **30** operating in parallel whose architecture is based on the processor developed by ITT Defense Communications Division for the Navy's Advanced Narrowband Digital Voice Terminal (ANDVT). The third processor identified as a control processor **31** is a Motorola 68000 which is used for control purposes. Control processor **31** interleaves the data, detects the presence or absence of received signals, interfaces to the other subsystems, and initializes and coordinates the operation of the modem functions just described with reference to FIGS. **3–8**. The various blocks of the modem subsystem are tied together by a common 68000 processsor **31** and data bus. Most of the activity on the bus is between the control processor and its memory. The bus also carries data between the various blocks. The bus has priority hardware for resolving conflicts when two or more requests for the bus occur simultaneously. This bus is identified as **32** in FIGS. **1** and **9**. Modem subsystem **1** also has a timing generator **33** (FIG. **1**). Timing generator **33** outputs are phase locked to the high precision frequency reference input from the controller subsystem **4**. Absolute time information is given to the modem via a packet timing epoch signal. The timing generator **33** then generates start of packet pulses, PN clocks, analog signal sample clocks, and data port clocks. The I/O (input-/output) circuit **34** (FIG. **1**) interfaces to the external control, data, PN ports, and to the input which provides error correction coding. This I/O circuit **34** also buffers the incoming and outgoing data and reads data from or stores data in the processor memory via direct memory access. Various components of circuit **34** of FIG. **1** are shown in FIG. **9** associated with the various processors **29–31**. Control processor **31** buffers the data arriving from the data ports and interleaves the data after it has been passed through the error correction coder/decoder **35**.

In the received path, control processor **31** deinterleaves the data and buffers the data between the decoding process and the output via coder/decoder **35**. Control processor **31** interfaces to controler subsystem **4** and to data ports for mode selection information, frequency hopping control data and data port handshaking signals (request to send, clear to send, and signal detect). Processor **31** also coordinates the two processors **29** and **30** by performing the following functions:

(1) allocating alternate packets of information to be operated on by the processors,

(2) combining information from both processors, and

(3) running doppler and time tracking loops.

Processors **29** and **30** perform the bulk of the calculations for modem subsystem **1**. Processor **29** performs the calculations for half of the packets (e.g., all of the even packets) and processor **30** operates on the other packets. Each processor **29** and **30** consists of an ANDVT processor and a DOT processor. The ANDVT/DOT processor is a programmable signal processor designed for speech and modem processing. FIG. **10** contains a general block diagram of the ANDVT/DOT processor. This processor has a Harvard architecture with separate program and data memories **36** and **37**, respectively. This two-bus structure enables parallel I/O operations such as loading multiplier **38** from data memory **37** while an input is read by the arithmetic logic unit **39**. The processor has a 330 nanosecond cycle time. For high data rate reception each ANDVT processor is augmented by a DOT processor which is optimized to perform complex multiply accummulations as shown in FIG. **10**. The DOT processor has a memory **40** which holds complex numbers. Control of the DOT processor, under direction of the ANDVT processor produces sequences of complex multiple accummulates in multipliers **40'**. Each multiply/accummulate cycle takes under 170 nanoseconds. Complex products are used in the modulation of the transmitted signal and in the demodulation of the received signal. The individual blocks of the modem subsystem **1** breaks the modem tasks into smaller and more easily handled functions. The combination of all the blocks in the modem subsystem **1** provides the capability to perform the required functions as outlined in FIGS. **3–8** and the flexability to handle new requirements that may arise.

As mentioned above, modem subsystem **1** functions are implemented using three programmable processors. Two processors **29** and **30** process alternate frames of data in the worst case receive mode. The third processor control processor **31** will act as interleave processor to interface the encoder/decoder **35** to the two processors **29** and **30**. Each processor **29** and **30** will have a hardware addition to provide the equalizer-cancellor processing requirements as shown at **41** and **42** of FIG. **9**. Control and status information I/O transfers will be split between the two processors **29** and **30**. Appropriate internal control and status information can then be transferred between the three processors through the bus **32**. Analog received Rx data is convereted to Rx symbols by processor **29** alone or alternately by frame, the Rx data is converted by Rx symbols by processors **29** and **30**. The Rx symbol data are then transferred to control processor **31** through bus **32**. Processor **31** performes the deinterleave algorithm on the received Rx

symbol data to produce Rx coded data which is then sent to the frequency hop-system controller subsystem 4. The transmit Tx data is processed through the same hardware except processor 30 is not used to convert Tx symbols to Tx samples.

Tx samples are generated by digital to analog conversion hardware in processor 29 only and are available through a coax connector at the back of the chassis 43.

Rx samples are received by analog to digital conversions hardware in processors 29 and 30 for alternate frame processing. The Rx Samples are available through a coax connector at the back of chassis 43. HW I/O are an extention of each processors 29 and 30 address and data bus. Through this connection, a processor 29 or 30 may transfer data, control, or status information between its hardware equalizer 41 or 42. Hardware equalizers 41 or 42 are functionally considered a part of processors 29 and 30, respectively. Equalizers-cancellers 41 and 42 contain I/O currents that enables an ANDVT processor to transfer data or control information between its hardware equalizer and other ANDVT, the interleave processor or the controller subsystem 4.

Control and status information between the controller susystem 4 and modem subsystem 1 is transferred via equalizer-canceller 41 and 42 which are controlled by processors 29 and 30. The control and status information can then be transferred between processors 29 and 30 or processor 31. Bus 43 enables transfer of control and status information between processors 29 and 30, processor 31 and controller subsystem 4. This bus also enables Tx/Rx coded data to be transferred between processor 31 and coder/decoder 35 and also enables Tx/Rx to be transferred between coder/decoder 35 and controler subsystem 4.

Processors 29 and 30 are programmable signal processors designed for speech and modem processing. It is augmented with a high-speed multiplier and general purpose programmability to satisfy the diverse requirements of digital signal processing computations. The entire design uses the minimum hardware possible and implements functions in software wherever it is consistent with performance requirements to maintain minimum power and size of the machine.

It should be noted that the high speed multiplier 38 (FIG. 10) is placed between the input and output buses to allow loading from either the data memory 37 or the arithmetic logic unit 39. This location is preferred to having multiplier 38 only after the data memory, because if the arithmetic logic unit 39 is the operand source the data must be first stored in memory. The reverse problem would exist if multiplier 38 was directly after the arithmetic logic unit 39. Program Memory 36 is a single-level microprogrammed implementation. All instructions are a single world in length. This allows branch addresses and literals to be immediately available without another memory cycle. The modest program lengths and the modem algorithms allow them to be programmed in one-chip depth of control memory (in a ROM version). This allows the single-level microprogramming.

FIG. 11 is a block diagram of the equalizer-cancellers 41 and 42 of FIG. 9. The I/O logic 45-47 includes straight forward implementation of buffers and registers to transfer data and control information between processors 29 and 30, control processor 31, equalizer cancellers 41 and 42 and controller subsystem 4. Equalizer-cancellers 41 and 42 are implemented with a pipeline architecture consisting of a 16×16 hardware multiplier 48, a 24×24 add/subtract logic 49 and a RAM I/O buffer and accummulator 50 controlled by a macro-micro sequencer 51. A single cycle is accomplished in 200 nanoseconds.

FIG. 12 shows a block diagram of control processor 31. Control processor 31 includes an 8 MHZ 68000 microprocessor 52, a program EPROM 53, a dynamic RAM data storage 54 parallel interface adapters 55 for interprocessor I/O dual RS 232 I/O 56 for development and diagnostic purposes and a serial I/O 57 for coded data transferred to and from coder/decoder 35.

The Modem subsystem 1 requirements call for a frequency hop modem to be used on a high frequency channel which may have severe multipath dispersions. In addition to frequency hopping, there is a requirement for a JR mode in which direct sequence spreading is used as well. A PN sequence modulation is required for spreading. PN sequences are also used for doppler and synchronization acquisition, equalizer training and addressing. Some of the latter functions are needed in the HDR mode (without spreading) as well.

A PN sequence correlates with itself but not with delayed versions of it when the delay is greater than a symbol interval. A long (24 hour) sequence has the greatest security but its correlation function fluctuates when the averaging interval consists of a small number of symbols. There are short (1 to 2 thousand symbols) PN sequences such as maximal length sequences, Gold sequences, etc. which can be generated by linear registers which have good correlation functions when the averaging interval is equal to one period of the sequences. A long PN sequence can be derived from a composite of a number of these shorter sequences. The composite sequence would have good correlation properties for averaging intervals equal to the length of the shorter composite sequences.

In modem subsystem 1, the averaging intervals are 32 symbols or longer, so that either approach for sequence generation is appropriate. The statistical fluctuations in the correlation function are relatively small with this large an averaging interval. The structure of modem subsystem 1 will permit generation of PN sequences from secure key generators, if desired. This does not preclude the use of linear shift registers sequences but simply does not make the architecture dependent on the properties of such specific sequences. Thus, except for the statistical fluctations due to the finite averaging interval, the PN sequence used for spreading, synchronization, and training, is assumed to have the correlation properties of the long random sequence mentioned above.

The frequency hopping requirement for the high frequency channel with multipath dispersion is a severe constraint on the design of the modem subsystem. The high frequency channel can be modeled as consisting of a small number of discrete propagation paths. The differential propagation delay between separate paths can be several milliseconds and this difference is referred to as multipath dispersion. In other words, if a narrow pulse, e.g., a symbol, is transmitted over the channel, multiple, delayed versions of it will be received. Furthermore, if a PN sequence is transmitted, multiple, delayed versions (echoes) of the sequence are received. The difference in delay between the received sequences can be many symbol periods in duration.

The PN sequences can be used to measure the impulse response of the channel. If the PN sequence is

transmitted and the received signal is correlated with a delayed version of the same PN sequence, the result is proportional to the channel impulse response corresponding to that delay time. By repeating the correlation with different values of delay, the channel impulse response can be measured. This impulse response characterizes the multipath dispersion of the channel. The use of a PN sequence minimizes the effect of noise and interference one the channel measurement.

The requirements of the modem subsystem 1 specifies a transmit bandwidth of 3 or 6 kHz, depending on the mode of operation. This is specified as a 99% power bandwidth. This requires that the transmit symbols be shaped by a transmit filter whose impulse response is significant for a number of symbol periods. This is further aggravated by the SSB filters in the RF subsystem 2. The overall impulse response seen at the receiver is a combination of the transmit filter, filters in the Rf subsystem 2 and the multipath dispersion. It is this overall impulse response that is measured by correlating with PN sequences.

Since this overall time dispersion extends for many symbol intervals, some means must be provided at the receiver to compensate for it. Equalization is one means for providing this compensation. Other approaches may also be used. All of these compensation methods require some form of channel measurement, e.g., equalizer training can be interpreted as channel measurement.

The severe problem posed by frequency hopping is due to the fact that the multipath dispersion is changing constantly with time and also is different from one frequency to another. The amplitude and phase of the signal received on an individual propagation path changes with time depending on the fine structure of the propagation conditions. This is known as fading (or multipath fading) an the rate at which it changes is called the fading rate. Individual echoes fade independently of each other. Wideband (greater than 10 kHz) channel measurement experiments (using, for example, PN sequence with symbol rates greater than 10 kHz) have been able to resolve individual echoes. In these experiments, it is found that the amplitude and phase of individual echoes are fairly constant (very low fading rate). However, with the bandwith constraints imposed on modem subsystem 1, the measured overall impulse response is not able to resolve individual propagation paths. When this happens, it is found that the individual echoes change much more rapidly with time (the fading rate is in the range of 1 to 10 Hz). This is due to the fact that now an echo is the resultant of adding several propagation paths, each with different amplitudes and phases. The resultant now changes very significantly due to small changes in phase of the individual components. This is the more commonly measured multipath fading seen with narrowband high frequency systems.

This is also the reason why the channel impulse response changes so significantly from one frequency to the next. The phase of the signal received over an individual propagation path is a sensitive function of the carrier frequency. If the carrier frequency changes (hops) the phases of the individual components all change randomly and the resultant echo amplitude and phase will be completely different from their values before the hop. Based on the requirements for the number of hop frequencies and for fading rate, it can be seen that it is not feasible to try to remember the channel impulse response for each particular frequency because, on the average, it will have changed more or less completely by the next time a particular frequency is reused.

The conclusion is that channel measurement (e.g., equalizer training) must be done independently on each frequency hop. This, combined with the fact that the receiver must compensate for mutipath dispersion that extends over many symbol intervals, puts stringent requirements on the modem subsystem 1 design approach. These considerations also result in requirements for processing capability in the modem subsystem implementation.

The processing capability needed for modem subsystem 1 implementation is determined primarily by the wider bandwidth (6 kHz) modes because the symbol rate and the number of symbols of multipath dispersions are both twice as great as the narrow bandwidth modes. In addition, the processing capability needs to be somewhat greater for the HDR mode because the information rate is higher requiring decisions on each symbol. Thus, the discussion that follows applies primarily to the HDR, 6 kHz, frequency hopping mode.

As discussed above, the requirements for frequency hopping on the high frequency channel with severe multipath distortion present stringent constraints on the design approach. Previous approaches to this problem have used DFE to compensate for the multipath dispersion of the high frequency channel. However, most, if not all, of these have been with frequency hopping. In addition, they have used a relatively small number of equalizer taps in comparison with the magnitude of the overall time dispersion imposed by the present requirements. For example, with the 5100 Hz symbol rate, the time dispersion is 25 symbols in duration which requires an equalizer with 25 feedback taps. Finally, the equalizer training techniques have been complex to implement.

The success of the narrow band high frequency terminal of the application depends upon a sound design approach for the modem subsystem 1 based on clear and well understood theory and implemented in a straightforward manner in which adequate processing capability is provided to insure that the approach determined by the theory is not compromised set forth herein.

As mentioned above, a high frequency modem has been developed for the Advanced Narrowband Digital Voice Terminal (ANDVT) which is implemented in software on a bit-slice signal processor. This hardware is similar to that used in the previous modem with decision feedback equalization mentioned above. Although the ANDVT high frequency model is a multitone modem and does not use equalization, the problems association with acquisition and tracking are similar to the present requirements. It has been found that a software implementation is essential for these sophisticated functions. On the other hand, even though the ANDVT processor has the capability to perform the decision feedback equalization with the number of taps used on previous high frequency modems, it does not have sufficient processing capability to meet the equalization requirements needed for the instant terminal. Therefore, it is proposed herein to augment the ANDVT processors with special purpose equalizer hardware 41 and 42 to perform the processing intensive equalizer functions.

The use of the existing ANDVT processor augmented with special-purpose hardware allows sophisticated real-time signal processing with substantial margin and also permits use of existing software routines and software developed support tools as applicable.

A recent series of papers Gersho, A. and Lim, T. L., "Adaptive Cancellation of Intersymbol Interference for Data Transmission," Bell System Technical Journal, Vol. 60, pp. 1997–2021, November 1981; Mueller, M. S. and Salz, J., "A Unified Theory of Data-Aided Equalization" Bell System Technical Journal Vol. 60, pp. 2023–2038, November 1981 and Foschini, G. J., and Salz, J., "Digital Communications Over Fading Radio Channels," Bell System Technical Journal, Volume 62, pp. 429–456, February 1983, clarifies the theory of optimum detection of data in the presence of noise and channel distortion. It further shows the relation of decision-feedback equalization to the optimal theory. One consequence of this theory for the present application is that the parameters for optimum processor to cancel channel distortion are easily obtained by channel measurement. Also, the theory of the optimum processor is easy to understand and to relate the processing requirements with the multipath dispersion. The pertinent aspects of this theory are summarized here.

The theory applies to the channel model discussed above. Symbols, which may be complex to represent multiphase data symbols, are transmitted through a transmit waveform shaping filter and then through the channel with multipath dispersion. The resultant signal along with additive, white noise is received at the modem input.

The optimum receiver consists of a linear filter matched to the overall impulse response (of the transmit filter and channel combined) followed by a linear canceller which removes intersymbol interference (ISI).

This has a satisfying interpretation. The matched filter maximizes the signal-to-noise ratio of the symbol to be detected. It effectively maximum ratio combines all of the individually-received echoes of that symbol which turns the multipath dispersion to a diversity-combining advantage. This is directly opposite to a linear equalizer which attempts to flatten the frequency response in effect enhancing the noise at places where the signal is weak.

The matched filter improves the signal-to-noise ratio of the desired symbol, but increases the ISI caused by adjacent symbols. However, the matched filter in the optimum receiver is followed by a linear canceller which subtracts out all ISI. Tnus, the optimum receiver has the performance of a system which sends only one symbol in which ISI is not a factor.

FIG. 13 shows the overall impulse response of the transmit filter and cnannel, h(t). For simplicity, it is shown as just a rectangular pulse with total time dispersion of MT seconds, where T is the symbol interval. The matched filter has impulse response $h^*(-t)$, where the asterisk denotes complex conjugate. FIG. 14 shows the overall impulse response of the transmit filter, channel and matched filter, r(t), which is just the convolution of h(t) with $h^*(-t)$. This has a total duration of 2MT seconds The output of the matched filter is sampled at the symbol rate in the optimum receiver. FIG. 14 illustrates the corresponding samples of r(t).

FIG. 15 illustrates the output of the matched filter when the transmit filter is driven by a symbol sequence a_n. Consider a sample of this output at time nT. The desired symbol appears at this time with amplitude $a_n r_o$. In addition, the sample will contain ISI terms due to symbols which precede and follow an There are a total of 2M ISI terms, M of which, $a_{n-M}r_M, \ldots, a_{n-1}r_1$, are postcursors due to symbols which precede a_n and M of which, $a_{n+1}r_{-1}, \ldots, a_{n+M}r_{-M}$, are precursors due to symbols which follow a_n. The linear canceller generates these ISI terms and subtracts them from the matched filter output sample prior to the symbol decision. Thus, the symbol decision is made on the desired symbol plus noise without ISI.

The optimum receiver is not realizable directly because it requires knowledge of the M symbols before and after the desired symbol to cancel the ISI. In practical receivers, prior decisions are used for these symbols. In this case, the only difference between the optimum and the practical receiver is due to the decision errors in these symbols. Practical approaches to linear ISI cancellation are discussed below.

The theory also determines a sub-optimum receiver which applies if the linear canceller has less then the 2M taps needed to cancel all of the ISI. This modification consists of a linear-transversal filter following the matched filter and preceding the linear canceller (which has a reduced number of taps). The tap spacing for the transversal filter is the symbol interval T.

The transveral filter has taps corresponding to the ones which have been deleted from the canceller. In this case, the tap gains for the transversal filter are determined to minimize the mean-square error between the transversal-filter output (less the ISI removed by the remaining canceller taps) and the desired symbol amplitude assuming the noise is present.

The sub-optimum receiver which results if the M precursor taps (corresponding to symbols following the desired symbol) are deleted from the linear canceller is equivalent to a decision feedback equalizer. This decision feedback equalizer is illustrated in block form in FIG. 16. FIG. 16 shows the matched filter 58 whose output is sampled at the symbol rate and the transversal filter 59 (of the sub-optimum receiver) which minimizes precursor ISI and noise. The feedback filter 60 is also a transversal filter with M taps to cancel the ISI from the M symbols following the desired symbol. It uses the prior symbols decisions to generate the postcursor ISI terms.

It is also possible to make a sub-optimum receiver in which the M postcursor taps are deleted from the linear canceller. This is illustrated in the decision feedforward equalizer of FIG. 17.

The equalizer-canceller in modem subsystem 1 and identified as 41 and 42 in FIG. 9 is shown in block diagram form in FIG. 6. It is intended that the equalizer-canceller process the received data in several passes. Therefore, the input data and output data is stored in buffer memory, such as buffers 61 and 62, so that it can be reused on each pass.

The first pass corresponds to the conventional decision feedback equalizer. In this case the switch 63 is in the down position so that the input data passes through transversal filter 64 which minimizes precursor ISI and noise (the parameter weights for this filter are not shown in FIG. 6). The feedback transversal filter 65 cancels the postcursors ISI using prior symbol decisions obtained in decision circuit 66. The resulting symbol decisions are stored in buffer 62 for the next pass.

At this point the process could stop. However, since now a complete set of symbol decisions exists in memory, the input dat can be passed through the equalizer-canceller. This time switch 63 is in the up position so that the system operates as a linear canceller, canceling both precursor and postcursor ISI. The weighting coefficients are the samples of the overall impulse response of the transmit filter, channel and matched filter, dis-

cussed previously and shown in FIG. 14. The coefficients for the canceller must be changed after the first pass to the values shown. The symbols and the coefficients will be complex in the proposed system. The second pass can be expected to produce fewer decision errors than the first pass because the prior decisions are used to cancel precursor ISI as well as postcursor ISI. In simulation experiments of a similar system the linear canceller produced as much improvement in performance over the decision feedback equalizer as the decision-feedback equalizer does over a linear (transversal) equalizer. Further passes can be expected to refine the decisions still further. The system of the application will be capable of at least three passes in realtime. Additional passes beyond three which are possible with the proposed hardware, will result in only marginal improvement.

A frequency hopping modem for the high frequency channel must perform equalizer training on each frequency hop as discussed previously. For the equalizer-canceller discussed hereinabove, this consists of channel measurement to determine the overall impulse response of the transmit filter and channel. From this information, the parameters of the matched filter, DFE and linear canceller must be calculated.

As discussed previously, the channel measurement is achieved by correlating the receive PN training signal with delayed versions of the PN sequence. This result is a sampled version of the impulse respnse h(t). The sampling interval for this impulse response and the matched filter is T/3, where T is the symbol interval.

The implementation of the matched filter will now be discussed. As already discussed, the output of the matched filter is sampled at the symbol interval T. These output samples are complex.

Although the matched filter output is sampled at the symbol interval T, the matched filtering operation itself must be done at a higher sampling rate which is consistent with the signal (and filter) bandwidth.

Systems described in the literature frequently take the form shown in FIGS. 18-22. FIG. 19 shows the bandpass spectrum of the received signal with the carrier frequency, fc, and Nyquist interval, 1/T, indicated. In this approach, quadrature mixers such as shown in FIG. 18 by mixers 67 and 68 are used to demodulate the carier signal to the low pass spectrum shown. In the low pass spectrum, the Nyquist interval is $\frac{1}{2}$T. Since practical systems use excess bandwidth (beyond the Nyquist interval), sampling must occur at a rate greater than 1/T. A sampling interval of T/2 is thus convenient. Complex samples are taken, as shown, in FIG. 18, where the real part of the sample is assumed to be the sample of the in-phase compoent and the imaginary part to be the quadrature sample.

The T/2 sample signal is passed through the low pass equivalent matched filter 69. The input and output samples of this filter are complex quantities. An output sample must be computed once every T seconds. Assuming the overall impulse response of the transmit filter and channel is MT seconds in duration, each output sample is the sum of 2M weighted input samples so that 2M/T complex or 8M/T real multiples per seocond are required for the matched filter.

A slightly different approach is used in the present arrangement. This approach samples the bandpass signal directly at the output of bandpass matched filter 70. Inspection of the bandpass receive spectrum shows that these samples must be at a rate greater than 2/T to accomodate the excess bandwidth (greater than the Nyquist interval). T/3 is a convenient sample interval, and as will be shown, leads to less processing than T/2 lowpass sampling.

FIG. 21 shows this T/3 approach. The matched filter is a bandpass filter 70 which is matched to the overall impulse response of the transmit filter and channel. The output of matched filter 70 is sampled once every T seconds to give the real sample of the output. In addition, the matched filter output of filter 70 is passed through a Hilbert transform 71 to generate the imaginary sample. This complex output sample is identical to the corresponding output sample in the lowpass approach of FIG. 18 except that it has been rotated by the carrier phase angle. This corresponds to the fact that these samples will represent the bandpass signal before demodulation. Retaining the carrier phase at this point is useful for doppler tracking.

FIG. 22 shows a slightly different approach to the bandpass matched filter arrangement of FIG. 21. Here, the upper transversal filter 72 represents the bandpass filter matched to the overall impulse response of the transmit filter and channel. Its output generates the real output samples at the output of adder 73. The lower transversal filter 74 is identical except that its coefficients have been transformed by a Hilbert transform. Its output therefore generates the imaginary output samples. For each (complex) output samples, 6M real multiples are required giving a total of 6M/T real multiplies per second. Thus, based on the number of multiples, this approach uses 25% less processing than the corresponding lowpass approach of FIG. 18. Actually, the approach of FIG. 22 has a greater savings because the lowpass filters used in the lowpass approach of FIG. 18 to remove the second harmonic components in the demodulator do not need to be implemented.

The terminal of FIG. 1 has stringenet requirements on the transmit symbol waveform shaping filter which is required to maintain the 99% power point bandwidth to 3 or 6 kHz. The transmit filter requirements are related to the symbol rate which should be as close to this allowed bandwidth as possible for maximum spread spectrum processing gain.

As discussed previously, the duration of the transmit filter impulse response adds to that of the channel multipath dispersion in determining the overall dispersion which must be equalized at the receiver. This overall dispersion has a major effect on the amount of processing required at the receiver for matched filtering and equalization.

In the wideband HDR mode, the data input consists of two 2400 bit/second data streams. These will be multiplexed into a single 4800 bit/second data stream before coding. The coder output will be a 9600 bit/-second stream rate which then goes into the interleave buffer. The interleave buffer transmits the data as a block consisting of a number of frequency hops (packets). Even with zero interleave depth, the coder output data is still transmitted in the form of packets in which the receiver maintains synchronization over each packet. Therefore, it is possible for the receiver to be able to identify individual bits in a block of data, either interleave blocks or packets.

This permits multiplexing of the two 2400 bits/-second data streams without additional overhead beyond that already used for packet synchronization. Packet synchronization and knowledge of packet number supplied by the Rf subsystem 2 permits the receive

modem to identify the relation of each receive symbol to the specific bits in the original 2400 bits/second data streams. Of course, this relation is complex because of the coding, interleaving, symbol encoding, frequency hopping, and decoder start-up and delay. However, the receiver knows where the desired receive data starts. Therefore, the demultiplexing of the two 2400 data streams can easily be achieved without special multiplexing overhead.

FIG. 23 is an enlarged block diagram of the Rf subsystem 2 which includes a transceiver 8 having therein an agile frequency synthesizer 75, programmable attenuator 76 associated with the power amplifier 9 and a Rf component box 77 included therein a voltage standing wave ratio bridge 78, agile low pass filter and power detector 10 and a T/R (transmit/receive) switch 79. Switch 79 is coupled to an optional antenna coupler 80 which is coupled to antenna 81. The components just named are under control of the interface and control circuit 82 which in turn is controlled by controller subsystem 4.

Referring to FIG. 24 there is illustrated therein a detailed block diagram of transceiver 8. The receiver input is coupled to a preselector 83 which is caused to select the low or high passband. The output of preselector 83 is coupled to mixer 84 receiving its frequency input from frequency synthesizer 75. Frequency synthesizer 75 has applied thereto a frequency control to provide either a single frequency output or a hopped frequency output. The output of mixer 84 is coupled to the first IF amplifier and filter 85 whose output is coupled to mixer 86 receiving a frequency input from a generator 87. The output of mixer is coupled to upper side band filter 87, lower side band filter 88 or the added channel for upper side band data 89 through adder 90. The output of filters 87 and 88 are coupled to second IF amplifiers and detectors 91 and 92, respectively, and, hence, to audio amplifiers 93 and 94 respectively. Channel 89 selects the 3 kHz or 6 kHz channel and applies the signal applicable thereto through filter 95 or 96 and applies the signals passed by filter 95 or 96 to adder 97, and hence, to second If amplifier and detector 98 whose output is coupled to data amplifier 99. The local oscilator signal for If amplifiers and detectors 91, 92 and 98 is provided by generator 100. The transmitter portion of the transcriber 8 includes the added channel data modulator 101 which includes data amplifier 102, data modulator 103 and the channel filters 104 and 105 whose outputs are coupled to adder 106. The output of adder 106 is coupled to adder 107. Other inputs to adder 107 are provided by audio amplier 108, modulator 109 and upper side band filter 110 and also audio amplifier 111, modulator 112 and lower side band filter 113. The adders 90, 97, 106 and 107, pass funcion like or gates and pass the appropriate signal to the appropriate channel, or in the case of adders 106 and 107 the signal of the active channel to the output of the adder 106 and 107.

The output of adder 107 is coupled to a mixer 114 which receives its local oscillator input from generator 87. The output of mixer 114 is passed to the first IF amplifier and filters 115 and, hence, to mixer 116 to raise the transmitter frequency to the desired frequency value and to hop the transmitted frequency when required. The output of mixer 116 is coupled to an automatic level control circuit 117 and, hence to wideband amplifier 118 to provide the exciter output.

FIG. 25 is a block diagram of agile frequency synthesizer 75 of FIGS. 1 and 24 and includes therein two frequency locked loops as shown therein labeled coarse loop 119 and output loop 120. The components of the frequency synthesizer are shown in FIG. 25 which operate in the usual fashion and, therefore, a detailed description of FIG. 25 is not believed to be necessary.

FIG. 26 is a detailed block diagram of the interface and control circuit 82 of FIGS. 1 and 23 with the components of this interface and control circuit and the operation thereof believed to be self-explanatory in view of the labeling of the various blocks and leads associated therewith and a detailed description thereof is not believed to be necessary.

FIG. 27 is a block diagram of controller subsystem 4. Controller subsystem 4 as illustrated in FIG. 27 allows the high frequency communication system to be operated from a central or a remote location for both fixed frequency and frequency-hopping modes of operation. With the exception of the packet timing module, all proposed nardware is available off-the-shelf. It is also almost entirely digital. This approach was adopted to allow maximum flexibility while minimizing design costs.

The crystal clock 121 and satellite synchronized clock 122 for timing syntnronization is currently being used with great reliability as is the frequency hopping mode of operation.

Controller subsystem 4 is an integrated microcomputer system that provides the facilities to operate the narrowband high frequency communication system in all its operational modes. Its primary building blocks are terminal processor 123, system timing generator 124, keyboard-display unit 125, cartridge tape drive 126, the aforementioned crystal clock 121 and satellite synchronization clock 122, message routing control module 127 and a printer (not shown).

After power turn-on terminal processor 123 will exercise a self-test sequence where proper operation of the system will be verified. The user will then be given the option to initialize the system either authomatically through the cartridge tape drive 126, or manually through the keyboard/display 125. The user is prompted for the correct input response. The input parameters are tested for validity with an appropriate error message being displayed when they are incorrect. Upon completion, and at any time thereafter, the user will be able to generate a new or updated cartridge tape for use in automatic initialization.

After initialization, the system reads the satellite synchronized clock 122 and waits for an authorized start time. One second before start time, the new PN sequence is computed for the PN generator. This generator is then flushed and the old PN sequences are replaced by the new Pn sequences. The system then readies itself for operation which commences with the next clock edge.

The operator will be presented a menu display of the system operational modes available and the keyboard input commands required to initiate them. Data inputs for the operational mode are entered through the console keyboard 125. The system prompts the operator via the console display 125 as to what information must be entered in order to properly exercise that mode. The system has a Control and Communication mode available. In the Control mode, the user is able to:

Select the system hopping frequencies
Select the Synchronization Preamble
Select the Interleaving Depth
Select the output power level

Select local or remote operaion of system
Select full or half-duplex operation
Exercise the system Built-In-Test

In the Communication mode, the user has the following modes of operation available:

SSB Voice
Low Data Rate - A/J
High Data Rate - no A/J

In the SSB Voice mode, the operator is able to enter the frequency and sideband directly from the keyboard (2.0 MHz to 30.0 MHz in 10 Hz increments, USB, LSB or ISB) or choose one of the allowable channels from a table of prestored frequencies. The RF subsystem **2** and in particular transceiver **8** is instructed to tune to that frequency. The remote microphone and speaker are connected to the transceiver and the operator is prompted to begin voice communication.

In the Low Data Rate - A/J mode the operator chooses either the Data or Source Encoded Voice mode of operation.

In the Data mode, the operator selects through interactive keyboard/display unit **25** the following:

Data rate
Packet rate/bandwidth
Mode
  Fixed Frequency
    Channel number
  Frequency Hopping
    Channels to use
    Select Call address to call

The system then instructs the transceiver to tune to the channel frequency in the fixed frequency mode or the hopping frequencies according to frequency hopping algorithm. The external Data Port **1** is connected to the Modem's Data Port **2** and the operator is prompted to begin data transmission.

In the Source Encoded Voice Mode (SEVM), the data rate and packet rate/bandwidth are fixed. The operator selects through interactive keyboard/display unit **125** the following:

Fixed frequency
  Channel number
    Frequency Hopping
  Channels to use
  Select call address to call

The system then instructes the transceiver to tune to the channel frequency in the fixed frequency mode or the hopping frequency according to the frequency hopping algorithm. The remote microphone and speaker are connected to the SEVM audio input, the Modem's Data Port **1** is connected to the SEVM's data port and the keyboard/display unit **125** is connected to the SEVM keyboard/display port. The Source Encoded Voice Module then prompts the operator on further inputs. This is all accomplished through necessary routing control module **127**.

In the High Data Rate - non-A/J mode the operator chooses either the Single Channel or Two Channel Data mode of operation.

In the Single Channel Data mode the packet rate/-bandwidth is fixed. The operator selects through interactive keyboard/display unit **125** the following:

Data Rate
  Mode
    Fixed Frequency
  Channel number
    Frequency hopping
  Channels to use
  Select call address to call

The system then instructs the radio or transceiver **8** to tune to the channel frequency in the fixed frequency mode, or the hopping frequency according to the frequency hopping algorithm. The external Data Port **1** is connected to the Modem's Data Port **1** and the operator is prompted to begin data transmission. This again is accomplished by module **127**.

In the Two Channel Data mode the packet rate/-bandwidth and data rate are fixed. The operator selects through the interactive keyboard/display unit **125** the following:

Mode
  Fixed frequency
Channel to use
  Frequency hopping
Channels to use
Select call address to call

The system then instructs transceiver **8** to tune to the channel frequency in the fixed frequency mode or the hopping frequencies according to the frequency hopping algorithm. Through module **127** the external Data Port **1** is connected to Modem's Data Port **1** and the external Data Port **2** is connected to the Modem's Data Port **2**. The operator is then prompted to begin data transmission.

The Terminal processor **123** is an integrated microcomputer system consisting of an Intel 86/30 single board computer and two 544 Intelligent Communications Controllers. The single board computer is centered around an 8086-2 central processing unit with a clock rate of 8 MHz. It contains 128K bytes of dual port RAM and up to 64K bytes of ROM. The Inteligent Communication Controllers contain an on board dedicated 8085A microprocessor providing communications control and buffer management for four programmable synchronous/asychronous channels.

The System timing generator **124** gives an on-off control of modem subsystem **1** and RF subsystem **2** for modular suppression during interpacket time in the frequency hopping mode. The fixed delays in transmit and receive timing signals provided by fixed delays **128** and **129** are provided to compensate for system filter delays in the transmit path between modem subsystem **1** and the RF subsystem **2** and in the receive path between RF subsystem **2** and modem subsystem **1**. A variable delay **130**, with a range of 0 to 10 milliseconds in 0.1 millisecond increments, is also provided in the receive timing signals path to compensate for any propagation delay between the spaced terminal sites.

The Interactive keyboard/display unit **125** (DEC VT-100) is the primary operator/system interface. It provides the user central control of all system modes and functions, and central viewing of all system indicators and error messages. All system modes are initiated by entering the appropriate commands through keyboard/display unit **125**.

Cartridge tape drive **126** (Cipher F420-30) provides the system with a mass storage devices for data input in automatic system initialization. It also enables the user to generate a new or updated initialization cartridge tape at any time during system operation.

Crystal clock **121** and satellite synchronized-clocks **122** combined provide the system with a stable time source for synchronous operation in the frequency hopping mode.

Crystal clock **121** (Austron 12100) with a frequency stability of $\pm 2 \times 10^{-10}$, is used by the system to gener-

ate precise timing signals for modem subsystem 1 and RF subsystem 2. It also acts as a reference frequency for satellite synchronized clock 122 which is used to update time automatically if satellite reception is lost. The portable crystal clock 121 is a self-contained time reference providing a stable time base for synchroniziing system timing and software interrupts. It contains a battery backup to maintain clock stability during power outages or during transport from one geographic location to another.

Satellite sychronized clock 122 (True Time Instruments 468-DC), continually updated by the NOAA "GOES" satellite, automatically provides the system NBS time to an accuracy of ±1.5 milliseconds. Clock 122 contains two satellite synchronized clocks whose components are hand matched to provide 50 microsecond timing correlation between the units when they are locked to the same satellite at the same location. A master synchronizing pulse, generated by satellite synchronized clock 122 synchronizes crystal clock 121 and, therefore, system timing, to within 0.4 microseconds of satelite synchronized clock 122.

Message routing control module 127 provides the automatic signal routing control necessary to operate the system in its various modes. After selection of the mode of communication through the interactive keyboard/display 125, the system sends control signals to message routing control module 127 to connect the system in its proper configuration.

A printer (DEC LA-120) (not shown) provides the user a hard copy of all test results during system automatic test sequences.

The operating software will provide the following:

Initialization

Self Testing

PN Generator

Operatin Control

System Input/Output

During initialization the controler subsystem 4 reads the initialization data from the cartridge tape drive 126, read the clock from the satellite synchronized clock 122 and seeds the PN Generator, and starts the hardware cycling.

During the self test the system will test RAM, ROM and central processing unit operation as well as system timing.

The PN Generator is a software shift register of sufficient length (greater than 25 bits) to have a repeat cycle of greater than 24 hours. The output and at least two other bit positions are MOD 2 summed to form the input to the shift register. The taps are chosen so that the characteristic polynomial of the register will produce a maximum length sequence.

The Operational Control is a software module that generates frequencies of the transmitter/receiver from the PN sequence, during frequency hopping operation. It provides the operator with user friendly promptly during mode seletion and parameter input, and provides output parameters to the subsystem modules for real time control during the system operation. It will poll the subsystems to determine status and alert the operator with approprate error messages during malfunctions.

The System Input/Output module packs the subsystem control information and provide it to the intelligent communication controllers of terminal processor 123 for output to the Subsystem Modules. The following Table I indicates I/O Data of controller subsystem 4:

TABLE I

DEVICE		DESCRIPTION	INPUT	OUTPUT
(1)	Modem Control	Data	(1) AGC Indication	(1) EPOC Number
			(2) Sync. Indication	(2) Frequency
			(3) Status	(3) Interleaving depth
			(4) Signal Quality	(4) Preamble sync. sel.
				(5) Bandwidth
				(6) Packet rate
				(7) Data rate
				(8) AJ/No AJ
				(9) FH/No FH
				(10) Callee address
				(11) Remote/Local
				(12) Exercise Bit
(2)	SEVM	Control Data	(1) Status	(1) Remote/Local
				(2) Exercise Bit
(3)	Transmitter Receiver	Control Data	(1) Status	(1) Frequency
				(2) USB, LSB or ISB
				(3) Output power level
				(4) AGC-level set
				(5) Bandwidth
				(6) Remote/Local
				(7) BIT
(4)	Data Set 1	Test Results	Data	—
(5)	Data Set 2	Test Results	Data	—
(6)	Keyboard Display	User Information	Keyboard Data	Display Data
(7)	Printer	Test Data	—	Data
(8)	External Time Source	Time	Data	—

TABLE I-continued

DEVICE	DESCRIPTION	INPUT	OUTPUT
(9) Message Routing Control	System Configuration	—	Data
(10) Antenna Coupler	Coupler Tuning Control	(1) Status (2) Forward Power (3) VSWR	(1) Frequency (2) Mode

while we have described above the principles of our invention in connection with specific apparatus it is to be clearly understood that this description is made only by way of example and not as a limitation to the scope of our invention as set forth in the objects thereof and in the accompanying claims.

We claim:

1. A spread spectrum communication system terminal comprising:

a first subsystem including

first means to encode locally generated digital data with an error correcting code,

second means coupled to said first means for spectrum spreading of said encoded locally generated digital data in at least one mode of operation of said communication system terminal,

third means to receive remotely generated error correcting code encoded digital data spectrum spread in said one mode of operation, and

fourth means coupled to said third means to recover said remotely generated digital data;

said encoded locally generated digital data and said encoded remotely generated digital data being processed in blocks of data bits, a second subsystem including

fifth means frequency hopping said encoded locally generated digital data prior to transmission to a remote location, and

sixth means frequency dehopping said encoded remotely generated digital data received from said remote location; and

a third subsystem including

seventh means coupled to said second means and said fifth means to provide a predetermined signal for spectrum spreading of said encoded locally generated digital data in said one mode of operation and to couple said encoded locally generated digital data to said fifth means, and

eighth means coupled to said third means, said fifth means said sixth means to provide a reference frequency for said frequency hopping and said frequency dehopping and to couple said frequency dehopped encoded remotely generated digital data from said sixth means to said third means,

said first means and second means including

a first processor coupled to said seventh means,

a first decision feedback equalizer/canceller coupled to said first processor, and

a second processor coupled to said first processor and said first decision feedback equalizer/canceller to provide said encoded locally generated digital data, said third means and said four means including

a third processor and said second processor coupled to said eighth means,

said first decision feedback equalizer/canceller coupled to said second processor,

a second decision feedback equalizer/canceller coupled to said third processor, and

said first processor coupled to said first and second decision feedback equalizer/canceller to recover said encoded remotely generated digital data,

said first, second and third processors operating according to predetermined data rate algorithms when said locally generated and remotely generated data rates are from 1200–4800 bits per second and spectrum spreading is not provided in the mode of operation of said communication system,

said first, second and third processors operating according to algorithms providing operation against jamming signals when said locally generated and said remotely generated data rates are below 1200 bits per second and spectrum spreading is provided in this mode of operation of said communication system.

2. A communication system according to claim 1, wherein

said predetermined signal for spectrum spreading is a pseudo noise sequence.

3. A communication system according to claim 2, wherein

said eighth means includes

a satellite synchronized clock continually updated by the NOAA "GOES" satellite, and

a crystal clock coupled to said satellite synchronized clock to provide said reference frequency.

4. A communication system according to claim 1, further including

a fourth subsystem including

ninth means coupled to said seventh means to provide locally generated low bit rate digital speech from a fixed coded vocabulary corresponding to recognized utterances for coupling to said fifth means, and

tenth means coupled to said eights means to receive remotely generated low bit rate digital speech from said sixth means to synthesize audio signals corresponding to said utterances at said remote location.

5. In a communication system employing frequency hopping and spread spectrum techniques, a modem subsystem comprising:

first means to encode locally generated digital data with an error correcting code,

second means coupled to said first means for spectrum spreading of said encoded locally generated digital data in at least one mode of operation of said communication system and to couple resultant digital data to a radio frequency subsystem for frequency hopping,

third means coupled to said radio frequency subsystem to receive remotely generated error correcting code encoded digital data spectrum spread in said one mode of operation and frequency dehopped in said radio frequency subsystem, and

fourth means coupled to said third means to recover said remotely generated digital data,

said first means and second means including

a first processor coupled to a controller subsystem,

a first decision feedback equalizer/canceller coupled to said first processor, and

a second processor coupled to said first processor and said first decision feedback equalizer/canceller to provide said encoded locally generated digital data,

said third means and said four means including

a third processor and said second processor coupled to said controller subsystem,

said first decision feedback equalizer/canceller coupled to said second processor,

a second decision feedback equalizer/canceller coupled to said third processor, and

said first processor coupled to said first and second decision feedback equalizer/canceller to recover said encoded remotely generated digital data,

said first, second and third processors operating according to predetermined data rate algorithms when said locally generated and remotely generated data rates are from 1200–4800 bits per second and spectrum spreading is not provided in the mode of operation of said communication system,

said first, second and third processors operating according to algorithms providing operation against jamming signals when said locally generated and said remotely generated data rates are below 1200 bits per second and spectrum spreading is provided in this mode of operation of said communication system.

6. A modem subsystem according to claim 5, wherein said encoded locally generated digital data and said encoded remotely generated digital data are processed in blocks of data bits.

7. A modem subsystem according to claim 6, wherein said spectrum spreading is accomplished by a pseudo-noise sequence.

8. A modem subsystem according to claim 7, further including

a timing generator coupled to said first, second and third processors under control of a system clock generator including

a satellite synchronized clock continually updated by the NOAA "GOES" satellite, and

a crystal clock coupled to said satellite synchronized clock to provide said reference frequency.

* * * * *

US005596601A

United States Patent [19]

Bar-David

[11] Patent Number: 5,596,601

[45] Date of Patent: Jan. 21, 1997

[54] **METHOD AND APPARATUS FOR SPREAD SPECTRUM CODE PULSE POSITION MODULATION**

[75] Inventor: **Israel Bar-David**, Haifa, Israel

[73] Assignee: **Lucent Technologies Inc.**, Murray Hill, N.J.

[21] Appl. No.: **298,260**

[22] Filed: **Aug. 30, 1994**

[51] **Int. Cl.**[6] **H04K 1/00**; H03K 7/04

[52] **U.S. Cl.** **375/207**; 375/200; 375/343; 375/239; 332/112; 370/213

[58] **Field of Search** 375/200, 207, 375/239, 343; 332/112; 329/313; 370/10, 8

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Primary Examiner—Stephen Chin
Assistant Examiner—T. Ghebretinsae

[57] **ABSTRACT**

A spread spectrum code pulse position modulated communication system is disclosed. The frequency spectrum of a transmitted signal is spread by encoding bits with a predefined spectrum-spreading codeword which is in accordance with regulatory requirements or other standardization decisions. When the predefined spread spectrum codeword is passed through a filter matched to the characteristics of the codeword, a peak is detected in the main lobe. A positive main lobe can indicate a binary value of "0" and a negative main lobe, associated with the inverse of the predefined codeword, can represent a binary value of "1". Additional information is conveyed by modulating the position of the center of the codeword within the symbol duration. In one embodiment, the position of the center of the codeword is varied among eight positions. Thus, eight signal states are available, and three additional bits may thereby be conveyed. Two differently and independently time-shifted spread spectrum codewords may be modulated, each with one of two orthogonal carrier signals, such as a sine and a cosine wave, thereby conveying a total of eight bits per symbol duration. Here, a symbol duration is the duration of a codeword.

20 Claims, 3 Drawing Sheets

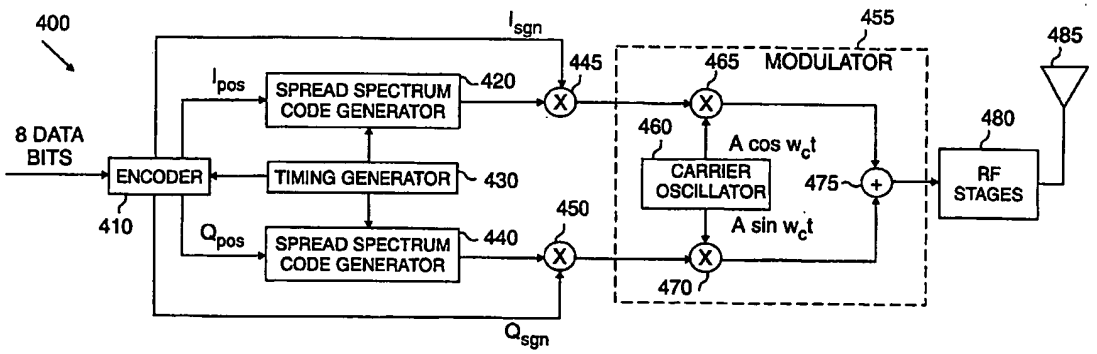
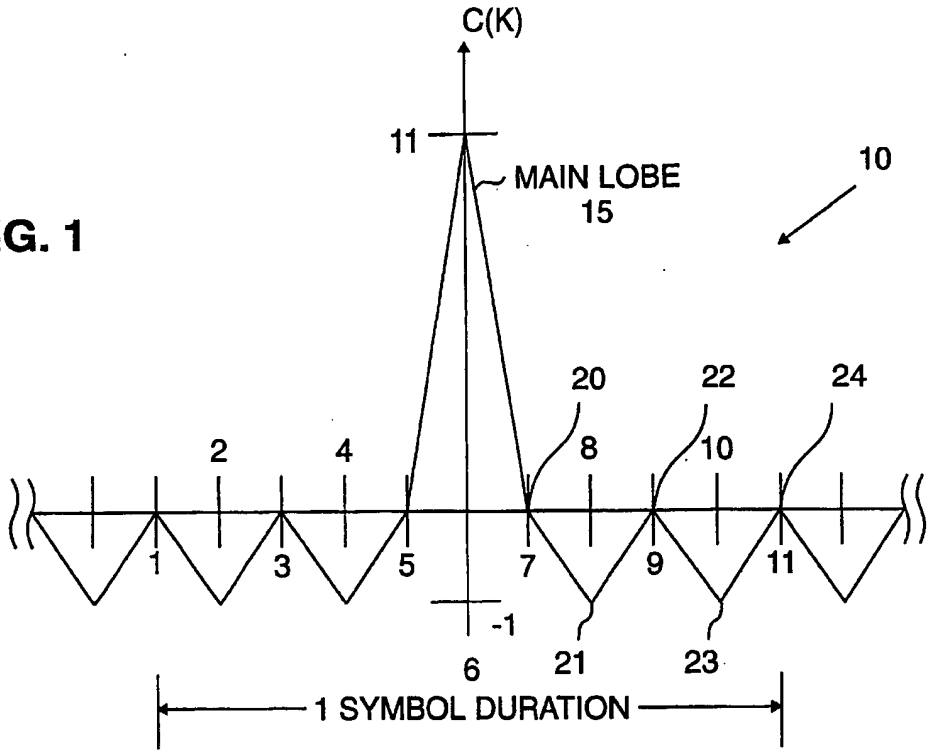


FIG. 1


C(K)
11
MAIN LOBE
15
10
20
22
24
2
4
8
10
1
3
5
7
9
11
-1
6
21
23
1 SYMBOL DURATION

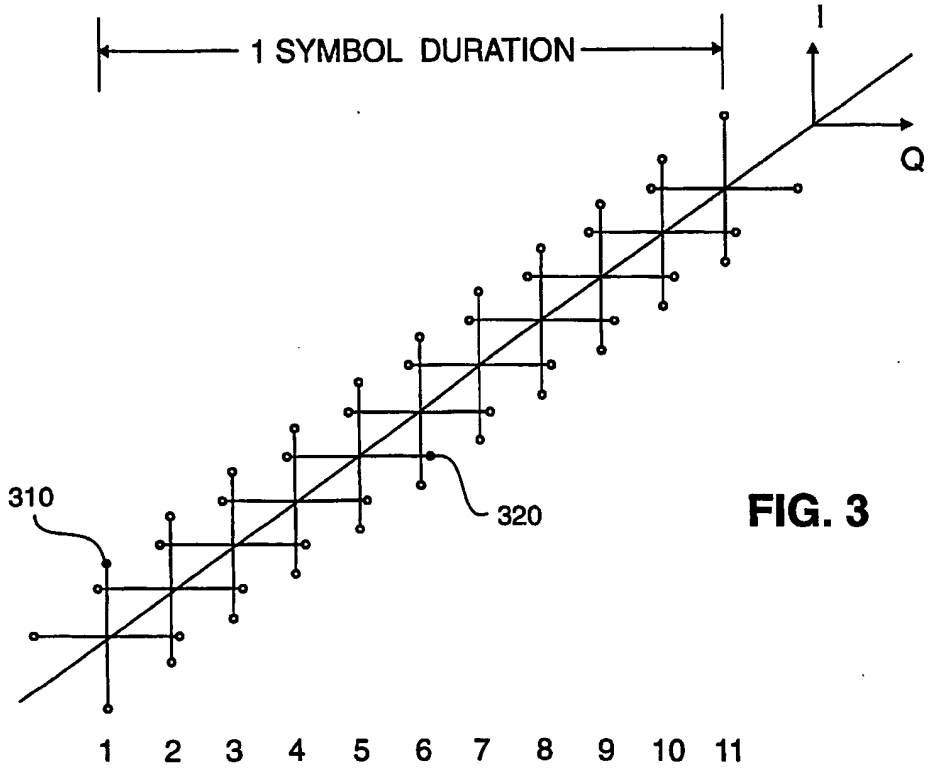
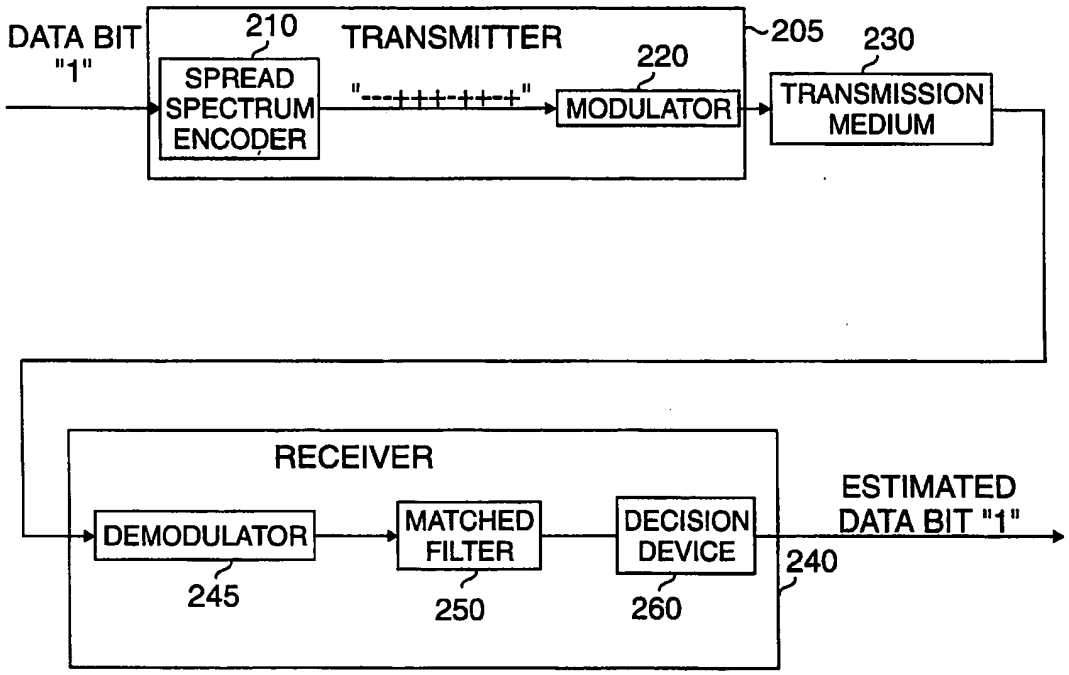

1 SYMBOL DURATION
I
Q
310
320
1 2 3 4 5 6 7 8 9 10 11

FIG. 3



PRIOR ART

FIG. 2

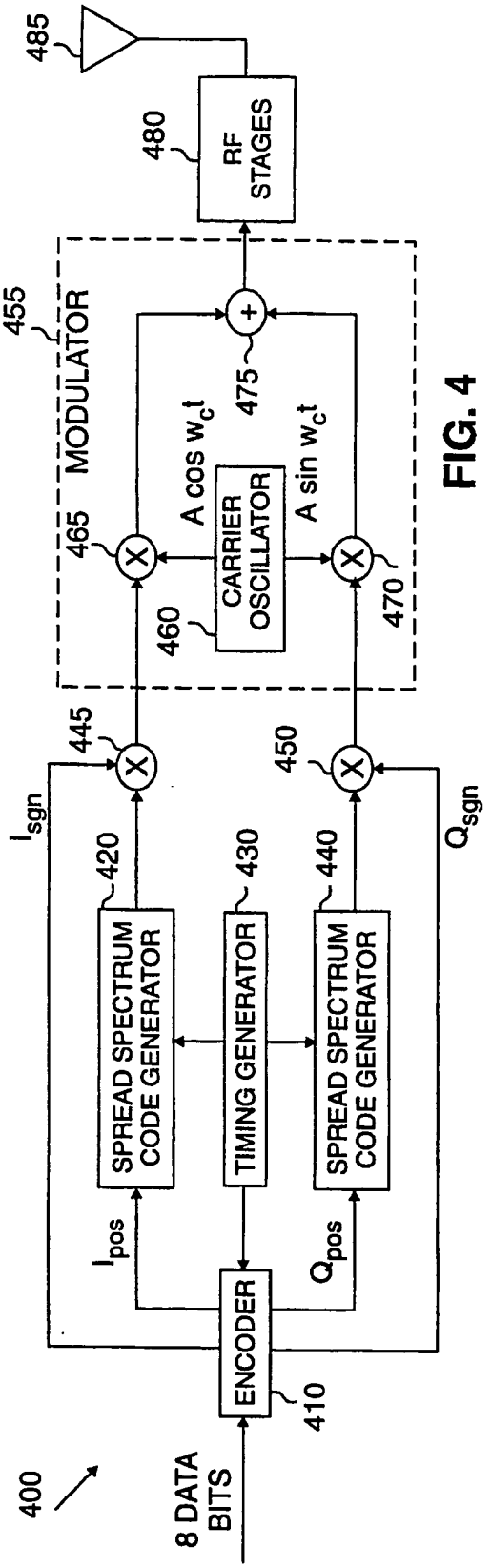

400
8 DATA BITS
ENCODER
410
SPREAD SPECTRUM CODE GENERATOR
420
TIMING GENERATOR
430
SPREAD SPECTRUM CODE GENERATOR
440
I_{pos}
Q_{pos}
I_{sgn}
Q_{sgn}
445
450
MODULATOR
455
465
460
CARRIER OSCILLATOR
470
A cos $w_c t$
A sin $w_c t$
475
RF STAGES
480
485

FIG. 4

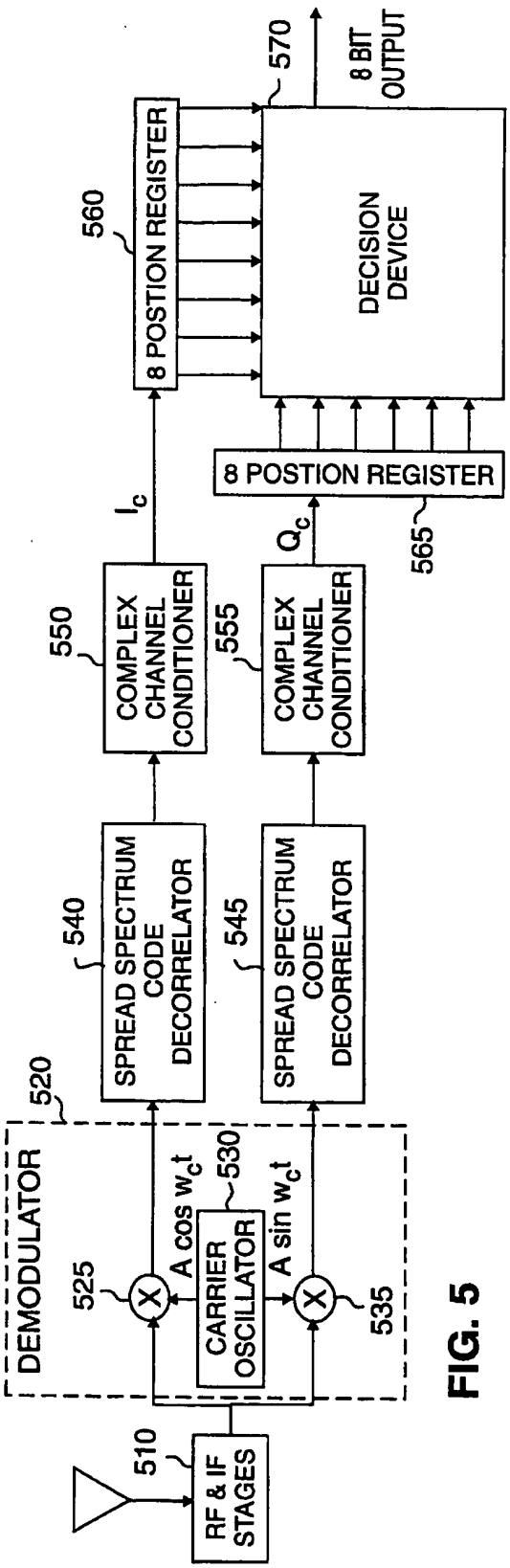

RF & IF STAGES
510
DEMODULATOR
520
525
CARRIER OSCILLATOR
530
535
A cos $w_c t$
A sin $w_c t$
SPREAD SPECTRUM CODE DECORRELATOR
540
SPREAD SPECTRUM CODE DECORRELATOR
545
COMPLEX CHANNEL CONDITIONER
550
COMPLEX CHANNEL CONDITIONER
555
I_c
Q_c
8 POSTION REGISTER
565
8 POSTION REGISTER
560
DECISION DEVICE
570
8 BIT OUTPUT

FIG. 5

METHOD AND APPARATUS FOR SPREAD SPECTRUM CODE PULSE POSITION MODULATION

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for modulation and demodulation of a communication signal, and more particularly, to a method and apparatus for modulation and demodulation of a communication signal where spectral spreading is desired.

BACKGROUND OF THE INVENTION

In many communication applications, it is often desired, or required, to spread the frequency spectrum of a transmitted signal by a given factor. For example, in the United States, the Industrial, Scientific and Medical (ISM) frequency band has historically been reserved for the operation of industrial, scientific and medical instruments. Recently, however, the Federal Communications Commission (FCC) has indicated that the ISM band may be utilized under certain conditions for communication applications, such as local area networks (LANs). Specifically, in order not to interfere with the operation of industrial, scientific and medical devices, the FCC requires that the frequency spectrum for communications in the ISM band be spread by a factor of at least 10. This is typically accomplished by encoding each bit to be transmitted using a predefined codeword, or pattern, consisting of at least 10 "chips" or "signal elements" which are all transmitted in the time frame normally allocated for a single bit.

The Institute for Electrical and Electronic Engineers has developed a standard for communications in the ISM band that utilizes the well known Barker code having a defined pattern of eleven chips, namely, "00011101101", as the basic information carrier. Thus, the Barker code may be utilized to represent a value of binary "0" and the inverse of the Barker code may be utilized to represent a value of binary "1", or vice-versa. Accordingly, for each transmitted eleven chip Barker code, one bit of information is conveyed.

Frequently, such spread spectrum systems will increase the bit rate by transmitting a number of bits during a single bit duration by utilizing phase-shift keying (PSK) modulation, wherein the phase of the carrier signal is shifted to represent data. In a quadrature phase-shift keying (QPSK) implementation, phase shifts in multiples of 90° are utilized. Thus, four possible signal states may be represented by each of the four phases. Accordingly, each signal element can represent two bits rather than one.

Although additional gains in the bit rate could be achieved by extending these phase shifting schemes, for example, to transmit three bits per signal element, by providing eight phase angles, the increase in transmission power that would be required to achieve adequate error rate performance presently makes such schemes impractical.

As is apparent from the above discussion of conventional spread spectrum modulation techniques, a need exists for a spread spectrum modulation technique that increases the number of bits that are transmitted per signal element without significantly adding to the power requirements of the transmitter.

SUMMARY OF THE INVENTION

Generally, according to one aspect of the invention, a communication system, suitable for use in frequency spreading applications, employs spread spectrum encoding to convey at least one bit of information per symbol duration, and conveys additional bits by modulating the position of the center of the transmitted spread spectrum codeword within the symbol duration which, upon matched filtering, modulates the position of the main lobe in the receiver output.

According to one feature of the invention, the frequency spectrum of the transmitted signal is spread in accordance with regulatory requirements or other criteria by encoding at least one bit of information with a predefined spread spectrum codeword. When the predefined codeword is passed through a filter matched to the characteristics of the codeword, a peak is detected in the main lobe. A positive main lobe can indicate a binary value of "0" and a negative main lobe, associated with the inverse of the predefined codeword, can represent a binary value of "1".

Another aspect of the invention will convey additional bits of information per symbol duration by modulating the position of the center of the codeword within the symbol duration. In one embodiment, the position of the center of the codeword may be manipulated within the defined symbol period by delaying the transmission of the codeword, by a positive or negative time period relative to the symbol duration. In one preferred embodiment, the position of the center of the codeword is varied among eight positions. Thus, eight signal states are available, thereby conveying three additional bits.

According to a further feature of the invention, additional bits may be conveyed by independently generating a plurality of time-shifted spread spectrum codewords and modulating each of the plurality of codewords with a carrier signal having a unique phase, amplitude or frequency. In one embodiment, two independently generated codewords are each modulated by an orthogonal carrier signal, such as a sine and a cosine wave, thereby conveying a total of eight bits per symbol duration.

A more complete understanding of the present invention, as well as further features and advantages of the invention, will be obtained by reference to the detailed description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a graphical illustration of the correlation function at the output of a matched filter for an eleven chip Barker Code;

FIG. 2 is a schematic block diagram illustrating an exemplary spread spectrum communication system in accordance with the prior art;

FIG. 3 is a graphical illustration of the modulation of the sign and position of the main lobe, upon matched filtering, for an eleven chip spread spectrum code;

FIG. 4 is a schematic block diagram of an illustrative spread spectrum position modulated transmitter according to the present invention; and

FIG. 5 is a schematic block diagram of an illustrative spread spectrum position modulated receiver according to the present invention.

DETAILED DESCRIPTION

The present invention provides a method and apparatus for modulating and demodulating a communication signal using spread spectrum encoding. The present invention improves on conventional spread spectrum modulation techniques by also modulating the position of the transmitted

spread spectrum code which, upon matched filtering, modulates the position of the main lobe in the receiver output. In this manner, additional information may be conveyed per symbol duration.

As previously indicated, it is often desirable, or required, to spread the frequency spectrum of a transmitted signal by a factor of n. This is typically accomplished by encoding each bit to be transmitted using a predefined codeword, or pattern, consisting of n "chips" or "signal elements" which are all transmitted in the time frame normally allocated for a single bit. In a preferred embodiment, often referred to as antipodal encoding, the predefined codeword may be utilized to represent a value of binary "0" and the inverse of the predefined codeword may be utilized to represent a value of binary "1". Alternatively, a bit of information can be conveyed by selecting from one of two predefined codewords.

A number of spread spectrum codes, consisting of a number of consecutive positive and negative signal elements, have been discovered which have unique properties that optimize the detection of the transmitted information. For example, a number of well known spread spectrum codes have been discovered by Barker, Neuman-Hofman, and Williard. For a discussion of these and other suitable spread spectrum codes, see Ning Zhan and S. W. Golomb, "Sixty Phase Generalized Barker Sequences," I.E.E.E. Trans. on Information Theory, Vol. 35, No. 4 (July, 1989), incorporated herein by reference.

The particular patterns for the spread spectrum codes are chosen such that when the pattern is detected at the output of a filter matched to the characteristics of the selected pattern, the amplitude of the main lobe is much greater than the amplitude of the side lobes. FIG. **1** illustrates the output **10** of a matched filter for the well known **11** chip Barker code, which has a pattern of "+++−−−+−+−", corresponding to a binary value of "0". Since the amplitude of the main lobe **15** is eleven times greater in magnitude than the amplitude of any side lobe, such as the side lobes **21** and **23**, the position of the main lobe **15** may be easily identified, even under possible change in polarity.

Accordingly, as shown in FIG. **2**, in order to transmit data using a conventional spread spectrum communication system **200**, each bit to be sent by a transmitter **205** is first encoded by a spread spectrum encoder **210**. Thus, if the encoder **210** is embodied as a Barker code generator, and a binary value of "1" is to be transmitted, the encoder **210** will generate a pattern of "−−−+++−+−+", which is the inverse Barker code. This information signal will then be modulated in a conventional manner by modulator **220** prior to transmission over a transmission medium **230**, which may be embodied as a conventional or wireless telecommunications network. The modulator **220** may employ a modulation technique, for example, which multiplies the codeword by a sinusoidal carrier wave in order to shift the signal frequency upward to the carrier frequency. In this manner, the original signal spectrum may be translated into a particular frequency band allocated by the FCC, or another regulatory body.

Upon receipt of the transmitted signal by the receiver **240**, the frequency of the received signal is first shifted down to the base band signal by a demodulator **245**, thus returning the signal to its original form prior to modulation. Thereafter, the received signal is passed through a filter **250** that is matched to the characteristics of the particular codeword. A decision device **260** will identify whether the peaks associated with the main lobes at the output of the matched filter **250** have a positive or negative value. A positive main lobe may indicate a binary value of "0", and a negative main lobe may be utilized to indicate a binary value of "1".

As previously indicated, conventional spread spectrum systems will frequently increase the bit rate by transmitting a number of bits during a single symbol duration by utilizing phase-shift keying (PSK) modulation, wherein the phase of the carrier signal is shifted to represent data. In a quadrature phase-shift keying (QPSK) implementation, phase shifts in multiples of 90° are utilized. Thus, four possible signal states may be represented by each of the four phases. Accordingly, each signal element can represent two bits rather than one.

In a conventional spread spectrum code implementation, four possible signal states are achieved by modulating two orthogonal carrier signals, such as a sine and a cosine wave, by a positive or negative spread spectrum codeword. Thus, the sine wave modulated by a positive codeword can represent a binary value of "1" of a first bit, and when modulated by a negative codeword can represent a binary value of "0". Similarly, the concurrently transmitted cosine wave modulated by a positive codeword can represent a binary value of "1" of a second bit, and when modulated by a negative codeword can represent a binary value of "0". Thus, two bits of information may be conveyed per bit duration.

It is noted that the cosine wave-modulated codeword is frequently referred to as the in-phase (I) signal, and the sine wave-modulated codeword is frequently referred to as the quadrature (Q) signal.

According to one feature of the present invention, the information rate that may be achieved with spread spectrum modulation techniques may be further increased by modulating the position of the main lobe associated with the transmitted codeword at the output of the matched filter.

As shown in FIG. **1**, for example, the eleven chip Barker code, upon matched filtering, will have a main lobe at position six that is one chip wide. Thus, additional information can be conveyed by manipulating the position of the main lobe, upon matched filtering, to appear in one of the other chip positions. If the position of the main lobe is varied among eight of the positions, eight signal states are available, and three additional bits may thereby be conveyed. Thus, one bit is conveyed by detecting the sign of the main lobe, and three additional bits are conveyed by detecting the position of the main lobe, for a total of four bits conveyed per symbol duration.

Further, in an implementation where the codeword is modulated by two orthogonal carrier signals, such as a sine and a cosine wave, as discussed above, a total of eight bits may thus be conveyed. Alternatively, a plurality of independently generated codewords may each be modulated by a respectively distinct carrier signal having a unique phase, amplitude or frequency. It is further noted that if a spread spectrum codeword having at least 16 chips is utilized, 16 signal states are available, and thus four additional bits of information could be conveyed for each codeword by modulating the position of the main lobe among 16 available positions.

FIG. **3** provides a graphical representation of the modulation of the sign and position for an eleven-chip spread spectrum code using two orthogonal carrier signals, I and Q. As previously indicated, in the illustrative embodiment, the position of the main lobe is manipulated to occupy one of eight available chip positions. Accordingly, the main lobe of the I signal may be positive or negative and occupy one of eight positions. Similarly, the main lobe of the Q signal may

be positive or negative and occupy one of eight positions. Bullet points **310** and **320** are utilized in FIG. **3** to indicate the sign and position of the I and Q signals. In the illustration of FIG. **3**, the I signal is positive, and is at location one, as shown by bullet point **310**, while the Q signal is positive and is at location five, as shown by bullet point **320**. As previously indicated, the illustrative embodiment may be utilized to convey eight bits of information.

In one embodiment, discussed further below, the position of the main lobe, upon matched filtering, may be manipulated within the defined symbol period by delaying the transmission of the codeword, by a positive or negative time period. Thus, in an implementation using an eleven chip codeword, if it is desired to position the main lobe in position **8**, rather than in position **6**, the natural position of the main lobe, the codeword generator should delay the transmission of the codeword by 2/11 of the symbol period. Similarly, if it is desired to position the main lobe in position **2** rather than in position **6**, the codeword generator should advance the transmission of the codeword by 4/11 of the symbol period.

It is noted that a common problem in many transmission media is the delay spread of the transmitted signal which results from the different arrival times of multiple signal components due to multipath propagation. For example, in a wireless local area network, signal components will have differential propagation times due to multipath propagation that results from rays bouncing off boundaries, such as walls and floors. As a result, it is not uncommon for a one microsecond pulse to spread to five microseconds.

Due to the delay spread of the received signal, some of the signal components of one bit position may spill over into other bit positions, causing intersymbol interference (ISI). The effects of delay spread are minimized by conventional equalizing techniques, discussed further below, which serve to "squeeze" the pulses into the proper symbol time.

It is also noted that when the transmission of a spread spectrum codeword is delayed relative to the symbol duration period, in order to modulate the position of the main lobe at the receiver output, in accordance with the present invention, some of the side lobes may actually spill over into an adjacent symbol duration period. However, since the amplitudes of the side lobes are much less than the amplitude of the main lobe, the interference on the adjacent symbols caused by the techniques of the present invention is negligible with respect to the interference that results from more conventional sources, such as the delay spread that results from multipath propagation.

In addition, when there are additional chip positions available which are not utilized to convey information, such as in the illustrative embodiment where only eight of the eleven available chip positions are utilized, the additional unused positions serve as a guard band or buffer for purposes of further minimizing intersymbol interference.

FIG. **4** is an exemplary implementation of a spread spectrum position modulated transmitter **400** in accordance with the present invention. In the exemplary transmitter **400**, the bits to be sent by the transmitter **400** are first encoded by an encoder **410**. For each 8 bit word to be transmitted, the encoder **410** will calculate the sign of the I and Q signals, I_{sgn} and Q_{sgn}; in other words, whether the I and Q pulses, respectively, should have positive or negative pulses. In addition, the encoder **410** will calculate the position of the I and Q signals, I_{pos} and Q_{pos}. It is noted that in the preferred embodiment, the values I_{pos} and Q_{pos} can be positive or negative time delay values, and indicate the time at which the respective spread spectrum code generators **420**, **440**, discussed below, should generate the spread spectrum code relative to the symbol duration period.

The encoder **410** and the spread spectrum code generators **420**, **440**, each operate according to the timing information that is received from the timing generator **430**, which will generate time pulses in accordance with the symbol duration period, as appropriate for the preselected spread spectrum codeword. Specifically, in the illustrative embodiment, the encoder **410** will read in eight data bits to be transmitted for each indicated symbol duration period.

Thereafter, the encoder **410** will calculate the I_{sgn}, Q_{sgn}, I_{pos} and Q_{pos} values, preferably in a Gray encoded manner. The encoder **410** preferably Gray-encodes in each coordinate, such that opposite binary input data sequences are allocated to opposite polarity Barker codes. For example, if the following sequences are allocated to I-position three and Q-position five, then the following sequences are allocated to:

Binary Sequence	I, O Polarity
00100100	+I, +Q
00100101	+I, −Q
00100110	−I, +Q
00100111	−I, −Q.

The spread spectrum code generators **420**, **440** will receive the appropriate time delay value, either I_{pos} or Q_{pos}, and will then generate the spread spectrum codeword in accordance with the calculated delay value, relative to the spread spectrum symbol interval center. In this manner, the main lobes of the I and Q signals will be shifted appropriately, in order to convey the desired information.

The time-shifted codewords generated by the spread spectrum code generators **420**, **440** will be multiplied by the polarity values indicated by the I_{sgn} and Q_{sgn} values, respectively, by the mixers **445** and **450**. Thus, the output of the mixers **445** and **450** will be the two information carrying signals, in other words, the positive or negative values of the time-shifted spread spectrum codeword, as appropriate.

The information carrying signals will then be modulated in a conventional manner by modulator **455** prior to transmission. The modulator **455** may employ a modulation technique, for example, which multiplies the I signal time-shifted codeword by a cosine wave using mixer **465**, and the Q signal time-shifted codeword by a sine wave using mixer **470**. In this manner, the signal frequencies of the original information signals are shifted upward to the carrier frequency associated with the carrier oscillator **460**, which may, for example, be in a particular frequency band allocated by the FCC, or another regulatory body.

The modulated I and Q signals will then be combined using an adder **475**, before passing through conventional RF stages **480**, which serve to amplify the modulated signals. Thereafter, the combined modulated I and Q signals may be transmitted over a transmission medium **485** to a receiver **500**, discussed below in conjunction with FIG. **5**. The transmission medium **485** may be embodied as a wired or a wireless telecommunications network.

FIG. **5** is an exemplary implementation of a spread spectrum position modulated receiver **500** in accordance with the present invention. In the exemplary receiver **500**, the frequency of the received signal first passes through RF and IF stages **510**, which serve to filter the received signal from the adjacent channel interference and to amplify the

received signal. Thereafter, the frequency of the received signal is shifted down to the base band signal by a conventional demodulator **520**, in order to return the received signal to its original form prior to modulation. In the illustrative embodiment, the I modulated signal is returned to baseband by multiplying it with a cosine wave, generated by carrier oscillator **530**, using mixer **525**, in order to isolate the I signal time-shifted codeword. In addition, the Q modulated signal is returned to baseband by multiplying it with a sine wave, using mixer **535**, in order to isolate the Q signal time-shifted codeword.

The demodulated I signal time-shifted codeword and the Q signal time-shifted codeword are then passed through spread spectrum code decorrelators **540** and **545**, respectively. The spread spectrum code decorrelators **540** and **545** are filters matched to the preselected codeword, in a known manner. Thus, the output of the spread spectrum code decorrelators **540** and **545** will be the correlation function of each signal, similar to the correlation function illustrated in FIG. **1** for an eleven chip Barker code. Due to the effects of delay spread, however, the main lobe and side lobes may be spread into the time period of an adjacent symbol, over the inherent spreading due to the Barker code side lobes themselves.

Accordingly, the I and Q signals are preferably conditioned by complex channel conditioners **550** and **555**, respectively, which serve to compensate for the delay spread of the communication channels, in a known manner. The complex channel conditioners **550** and **555** may be embodied as a complex equalizer, of known type, or as filters which are matched to the particular delay spread characteristics of the communication channel, for example, by measuring the channel impulse by using a preamble signal before transmitting the data.

The conditioned I and Q signals, I_c and Q_c, may then be analyzed to identify the sign and the position of each main lobe. In the illustrative embodiment, the eight chip positions of the I and Q signals that are utilized to convey information are preferably sampled and stored using eight-position registers **560** and **565**, respectively. Thus, each position of the register **560**, **565** will contain the amplitude value of the corresponding chip position of the I and Q signals.

Thereafter, the values stored in the positions of the registers **560** and **565** are analyzed by a decision device **570** in order to detect the sign and position of the main lobes of the I and Q signals and translate this information into the appropriate eight bit binary word. In a preferred embodiment, the decision device **570** identifies the sign and position of the main lobe of the I and Q signals by selecting the largest stored amplitude value in each of the registers **560** and **565**, respectively. As previously indicated, in the illustrative embodiment, the sign of the main lobe of the I signal conveys one bit, and the position of the main lobe conveys an additional 3 bits. Similarly, the sign of the main lobe of the Q signal conveys one bit, and the position of the main lobe conveys an additional 3 bits. Thus, a total of eight bits of information are conveyed.

It is noted that where residual coupling occurs between the I and Q signals, the coupling coefficients can be taken into account in a more complex decision device **570**.

It is to be understood that the embodiments and variations shown and described herein are illustrative of the principles of this invention only and that various modifications may be implemented by those skilled in the art without departing from the scope and spirit of the invention.

We claim:

1. An apparatus for transmitting information across a communication channel, said apparatus comprising:

a first spread spectrum code generator for generating a first or second spread spectrum codeword to convey at least one bit of information, said codewords consisting of a plurality of chips transmitted during a symbol duration, said codewords having a main lobe in one of said chip positions upon matched filtering in a receiver;

said first spread spectrum code generator further comprising a means for modulating the position of said codeword generated by said first spread spectrum code generator relative to the center of said symbol duration to modulate the position of said main lobe in said receiver output to convey one or more additional bits of information;

a first carrier signal source;

a modulator connected to said first spread spectrum code generator and said first carrier signal source, said modulator generating a first carrier signal modulated by said generated codeword having its position modulated relative to the center of said symbol duration; and

means for applying said modulated carrier signal to an input of said communication channel.

2. The transmitter apparatus of claim **1**, further comprising:

a second spread spectrum code generator for generating a third or fourth spread spectrum codeword to convey at least one bit of information;

said second spread spectrum code generator further comprising a means for modulating the position of said codeword generated by said second spread spectrum code generator relative to the center of said symbol duration to modulate the position of said main lobe in said receiver output to convey one or more additional bits of information;

a second carrier signal source, said second carrier signal being distinguishable from said first carrier signal; and

said modulator connected to said second spread spectrum code generator and said second carrier signal source, said modulator generating a second carrier signal modulated by said codeword generated by said second spread spectrum code generator and having its position modulated relative to the center of said symbol duration.

3. The transmitter apparatus of claim **1**, wherein said second spread spectrum codeword is the inverse of said first spread spectrum codeword.

4. The transmitter apparatus of claim **2**, wherein said fourth spread spectrum codeword is the inverse of said third spread spectrum codeword.

5. The transmitter apparatus of claim **1**, wherein said communication channel is a wireless radio channel.

6. The transmitter apparatus of claim **1**, wherein the frequency of said first carrier signal is in the Industrial, Scientific and Medical frequency band.

7. An apparatus for receiving a plurality of bits of information transmitted across a communication channel, one or more of said received bits being encoded using a first or second spread spectrum codeword transmitted during a symbol duration to convey at least one bit of information, said generated codeword having a main lobe upon matched filtering, one or more additional received bits being encoded by shifting the position of said generated codeword relative to the center of said symbol duration to modulate the position of said main lobe upon said matched filtering, said receiver apparatus comprising:

a filter matched to said first and second spread spectrum codewords;

means for analyzing said filter output to detect the polarity and position of said main lobe relative to the center of said symbol duration; and

means for analyzing said polarity and position information of said main lobe to decode said transmitted data.

8. The receiver apparatus of claim **7**, further comprising a complex channel conditioner which essentially compensates for the delay spread of said communication channel.

9. The receiver apparatus of claim **7**, wherein said second spread spectrum codeword is the inverse of said first spread spectrum codeword.

10. The receiver apparatus of claim **7**, wherein said communication channel is a wireless radio channel.

11. A communication system comprising:

a transmitter for encoding data using a spread spectrum codeword to convey at least one bit of information, said codeword consisting of a plurality of chips transmitted during a symbol duration, said codeword having a main lobe in one of said chip positions upon matched filtering, said transmitter further including means for shifting the position of said generated codeword relative to the center of said symbol duration to modulate the position of said main lobe upon said matched filtering to convey one or more additional bits of information;

a receiver including a filter matched to said codeword, said receiver further including means for analyzing said filter output to detect the polarity and position of said main lobe to decode said transmitted data; and

a communication channel for connecting said transmitter and receiver.

12. The communication system of claim **11**, wherein said communication channel is a wireless local area network.

13. A method for transmitting data across a communication channel, said transmission method comprising the steps of:

generating a first or second spread spectrum codeword to convey at least one bit of information, said codewords consisting of a plurality of chips transmitted during a symbol duration, said codeword having a main lobe in one of said chip positions upon matched filtering in a receiver;

modulating the position of said generated codeword relative to the center of said symbol duration to produce a modulated codeword in which the position of said main lobe in said receiver output is employed to convey one or more additional bits of information;

generating a first carrier signal;

modulating said first carrier signal using said modulated codeword; and

applying said modulated carrier signal to an input of said communication channel.

14. The transmission method of claim **13**, further comprising:

generating a third or fourth spread spectrum codeword to convey at least one bit of information;

modulating the position of said generated codeword relative to the center of said symbol duration to produce a modulated codeword in which the position of said main lobe in said receiver output is employed to convey one or more additional bits of information;

generating a second carrier signal, said second carrier signal being distinguishable from said first carrier signal; and modulating said second carrier signal using said modulated codeword.

15. The transmission method of claim **13**, wherein said second generated codeword is the inverse of said first generated codeword.

16. The transmission method of claim **14**, wherein said fourth generated codeword is the inverse of said third generated codeword.

17. The transmission method of claim **13**, wherein said communication channel is a wireless radio channel.

18. A method for receiving a plurality of bits of information transmitted across a communication channel, one or more of said received bits being encoded using a first or second spread spectrum codeword transmitted during a symbol duration to convey at least one bit of information, said codeword having a main lobe upon matched filtering, one or more additional received bits being encoded by shifting the position of said generated codeword relative to the center of said symbol duration to modulate the position of said main lobe upon said matched filtering, said method for receiving comprising the steps of:

filtering said received signal using a filter matched to said spread spectrum codewords;

analyzing said filter output to detect the polarity and position of said main lobe relative to the center of said symbol duration; and

analyzing the polarity and position of said main lobe to decode said transmitted data.

19. The receiver method of claim **18**, further comprising the steps of conditioning said filtered signal using a complex channel conditioner which essentially compensates for the delay spread of said communication channel.

20. The receiver method of claim **18**, wherein said communication channel is a wireless radio channel.

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US006473449B1

(12) **United States Patent**
Cafarella et al.

(10) **Patent No.: US 6,473,449 B1**
(45) **Date of Patent: Oct. 29, 2002**

(54) **HIGH-DATA-RATE WIRELESS LOCAL-AREA NETWORK**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/487,395**

(22) Filed: **Jan. 18, 2000**

Related U.S. Application Data

(63) Continuation of application No. 09/048,651, filed on Mar. 26, 1998, now Pat. No. 6,075,812, which is a continuation of application No. 08/369,778, filed on Dec. 30, 1994, now Pat. No. 5,809,060, which is a continuation-in-part of application No. 08/198,138, filed on Feb. 17, 1994, now abandoned.

(51) **Int. Cl.**[7] **H04L 27/30**; H04B 15/00; H04K 1/00; H04J 3/16; H04J 3/22

(52) **U.S. Cl.** **375/141**; 375/130; 375/200; 370/471

(58) **Field of Search** 375/141, 200, 375/130; 370/471

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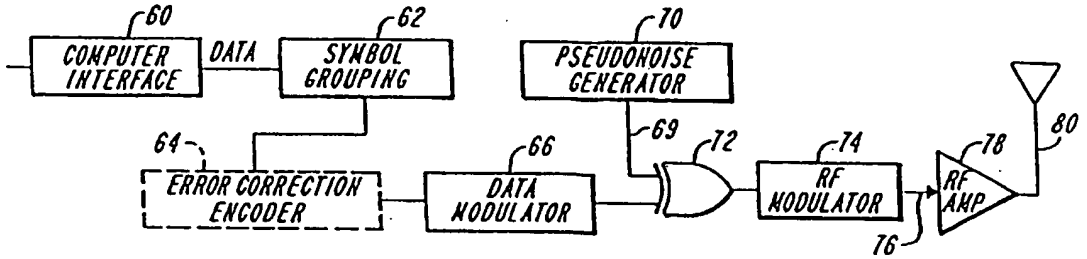
(57) **ABSTRACT**

An apparatus and method for communicating data between at least two data devices, suitable for use as a wireless local-area network, that provides robust data communication via a radio communications channel corrupted by multipath interference, particularly at high data rates. A preferred embodiment of the invention represents data as a sequence of Walsh-function waveforms encoded by pseudo-noise direct-sequence spread-spectrum modulation. Walsh-function-encoding of the data provides a long symbol duration, thereby allowing the spread-spectrum modulation to provide processing gain sufficient to substantially overcome multipath interference, while providing a high data rate. In another preferred embodiment, Walsh-function modulation is supplemented with various forms of phase modulation, such as coherent PSK for bi-orthogonal signalling, and DPSK between orthogonal symbols for non-coherent bi-orthogonal signalling, thereby further increasing data rate without reducing processing gain. In another preferred embodiment, Walsh-function modulation is supplemented with spectral shaping to allow increased bandwidth occupancy, thereby further increasing the processing gain without sacrificing data rate.

43 Claims, 16 Drawing Sheets



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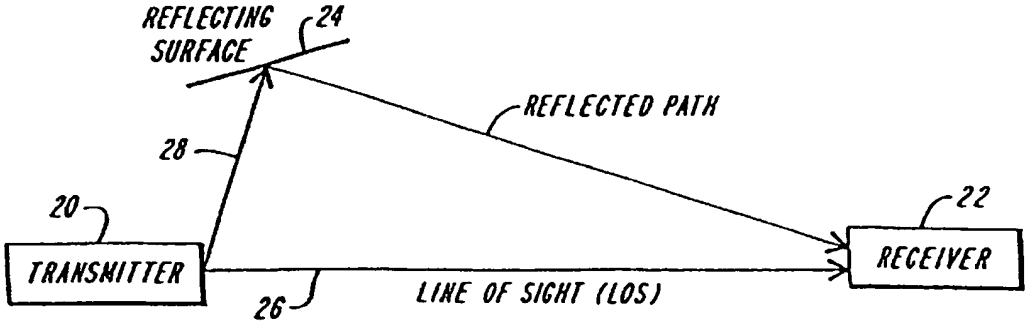

FIG. 1

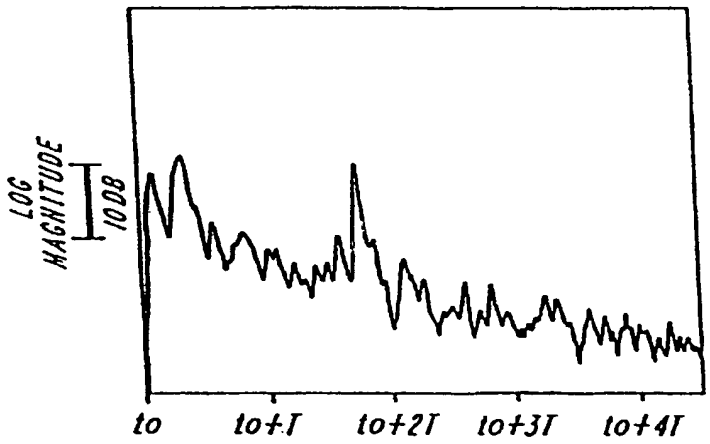

FIG. 2

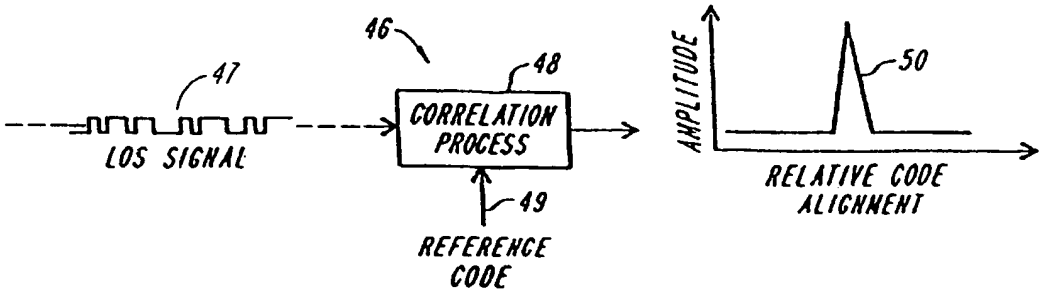

FIG. 4

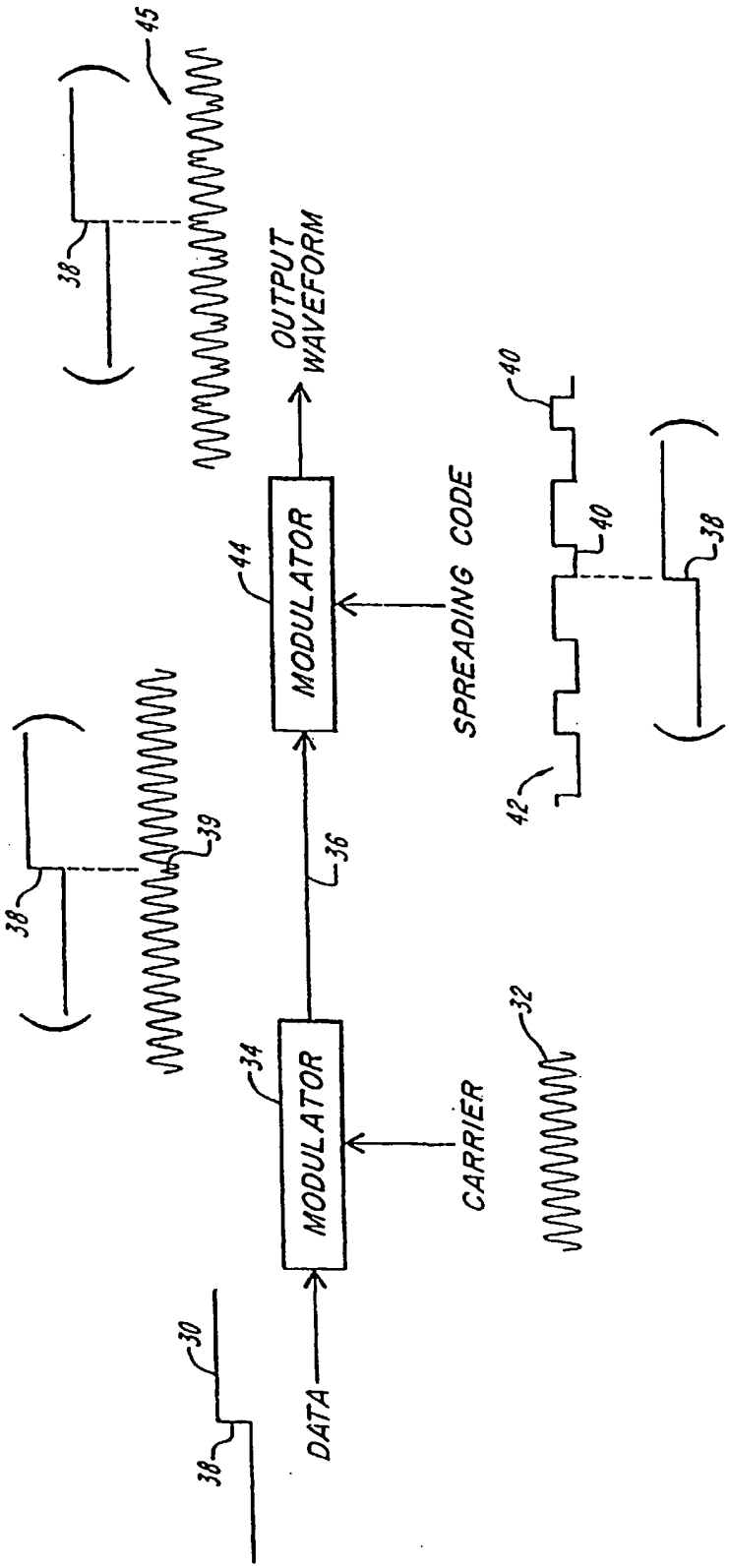
45
38
OUTPUT WAVEFORM
44
MODULATOR
SPREADING CODE
40
40
38
42
38
39
36
38
34
MODULATOR
CARRIER
32
30
38
DATA

FIG. 3

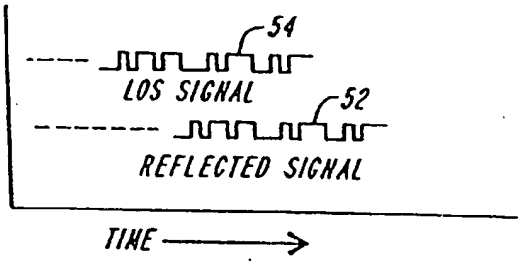

FIG. 5A

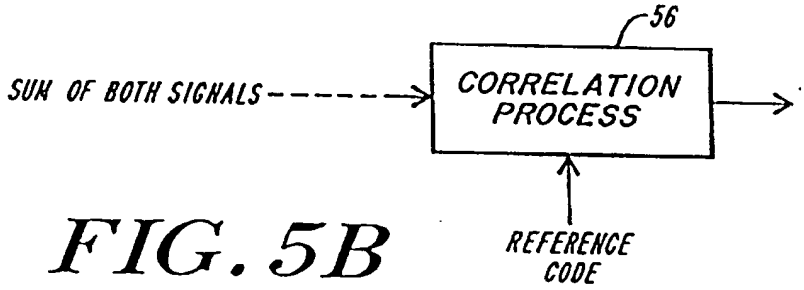

FIG. 5B

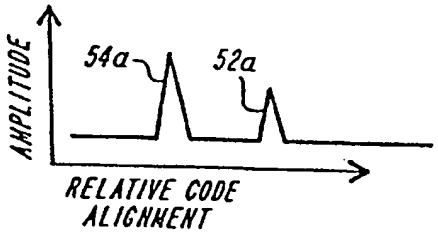

FIG. 5C

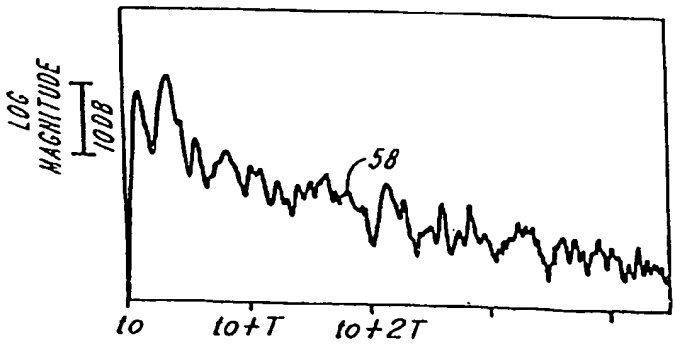

FIG. 6

REQUIRES FAST SYNCHRONIZER ?			
	MESSAGE-SWITCHED	PACKET-SWITCHED	
		LONG	SHORT
TIME-SLOTTED	NO	NO	NO
RANDOM	NO	NO	YES

FIG. 7

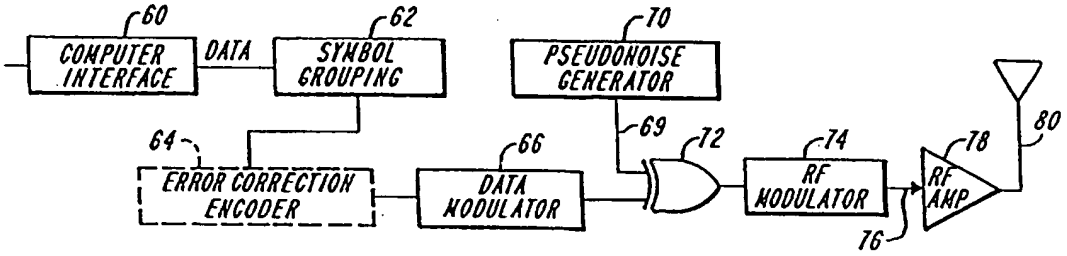

FIG. 8

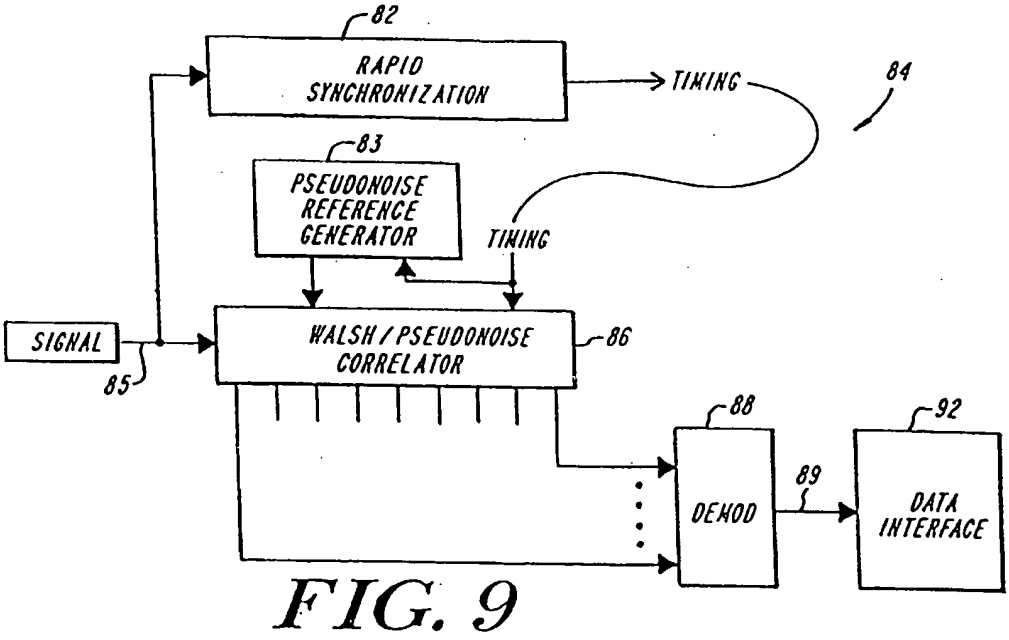
82
RAPID SYNCHRONIZATION
TIMING
84
83
PSEUDONOISE REFERENCE GENERATOR
TIMING
SIGNAL
85
WALSH / PSEUDONOISE CORRELATOR
86
88
DEMOD
89
92
DATA INTERFACE

FIG. 9

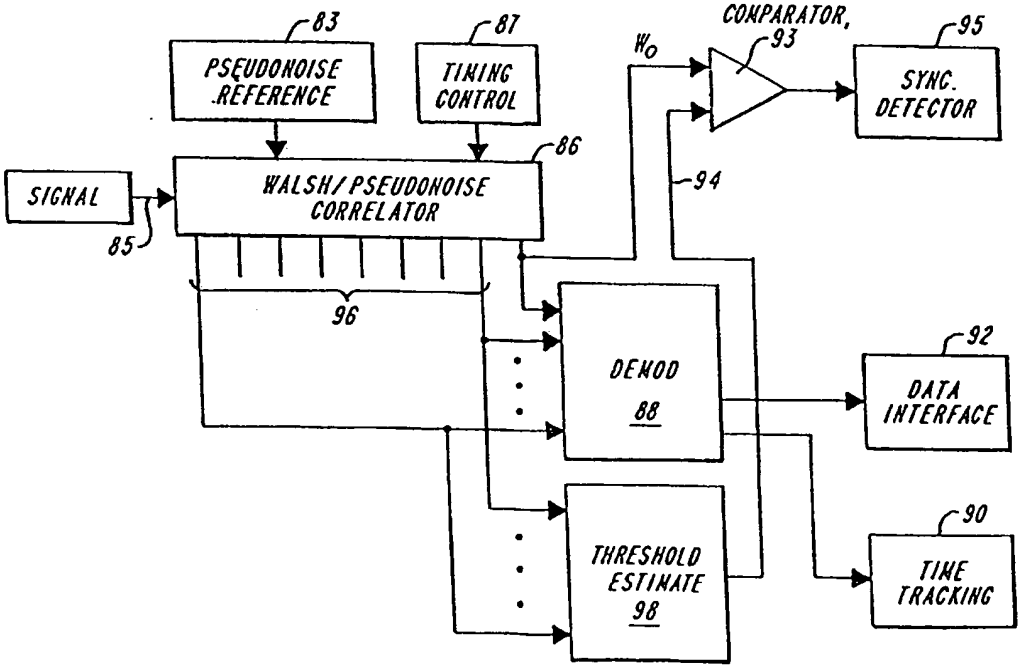
83
PSEUDONOISE REFERENCE
87
TIMING CONTROL
86
SIGNAL
85
WALSH/PSEUDONOISE CORRELATOR
96
W_0
COMPARATOR, 93
95
SYNC. DETECTOR
94
DEMOD 88
92
DATA INTERFACE
THRESHOLD ESTIMATE 98
90
TIME TRACKING

FIG. 10

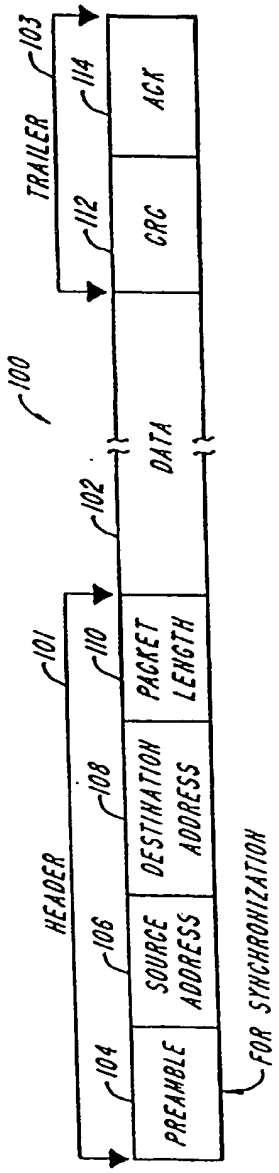
100
HEADER
101
TRAILER
103
PREAMBLE
104
SOURCE ADDRESS
106
DESTINATION ADDRESS
108
PACKET LENGTH
110
DATA
102
CRC
112
ACK
114
FOR SYNCHRONIZATION

FIG. 11

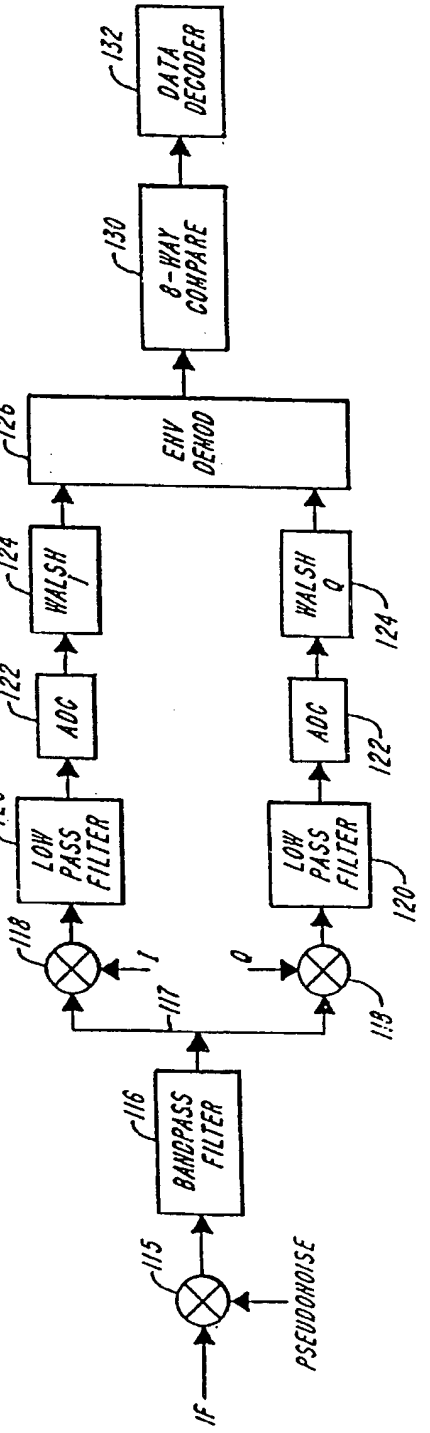
IF
PSEUDONOISE
115
BANDPASS FILTER
116
117
I
Q
118
119
LOW PASS FILTER
120
ADC
122
WALSH I
124
WALSH Q
124
ENV DEMOD
126
8-WAY COMPARE
130
DATA DECODER
132

FIG. 12

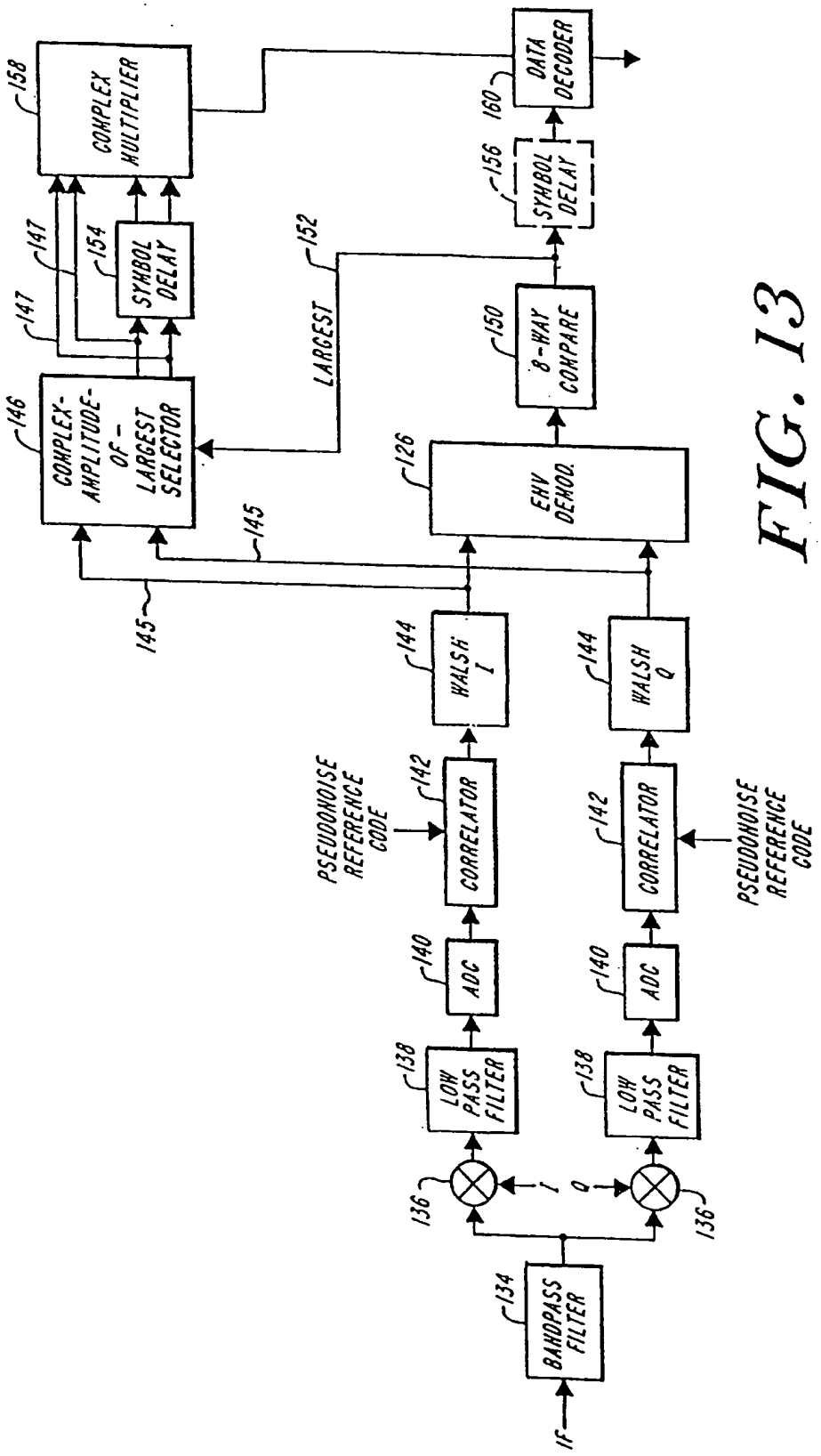
IF
BANDPASS FILTER
134
136
I
Q
LOW PASS FILTER
138
ADC
140
CORRELATOR
142
PSEUDONOISE REFERENCE CODE
WALSH I
144
WALSH Q
144
145
EHV DEMOD.
126
8-WAY COMPARE
150
LARGEST
152
SYMBOL DELAY
156
DATA DECODER
160
COMPLEX MULTIPLIER
158
SYMBOL DELAY
154
147
147
COMPLEX-AMPLITUDE-OF-LARGEST SELECTOR
146
145

FIG. 13

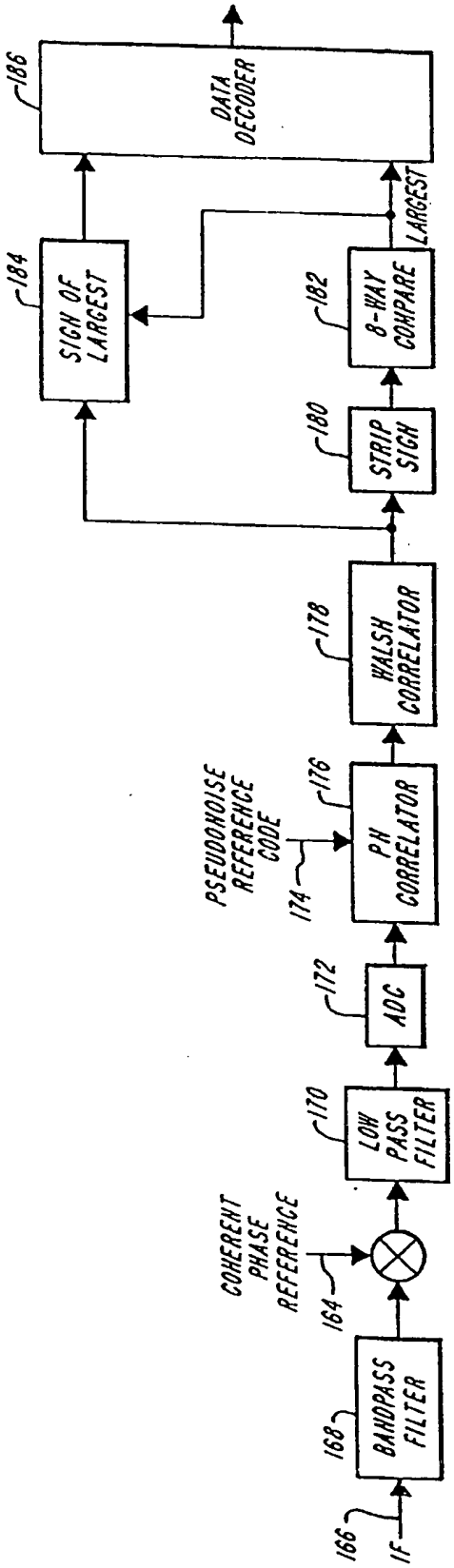
IF
166
BANDPASS FILTER
168
COHERENT PHASE REFERENCE
164
LOW PASS FILTER
170
ADC
172
PSEUDONOISE REFERENCE CODE
174
PN CORRELATOR
176
WALSH CORRELATOR
178
STRIP SIGN
180
8-WAY COMPARE
182
LARGEST
SIGN OF LARGEST
184
DATA DECODER
186

FIG. 14

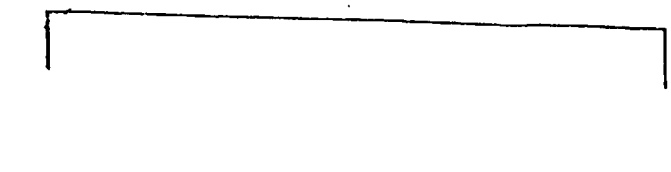

FIG. 15A

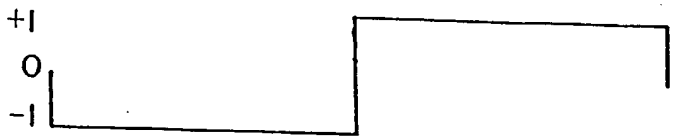

FIG. 15B

FIG. 15C

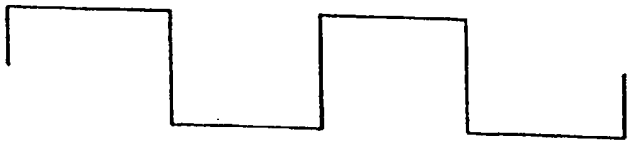

FIG. 15D

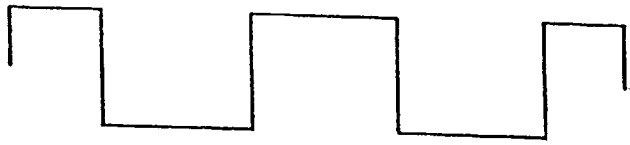

FIG. 15E

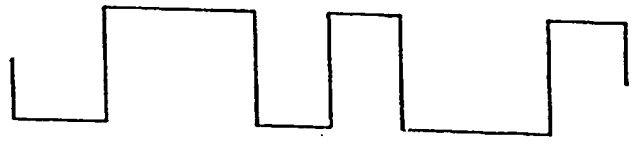

FIG. 15F

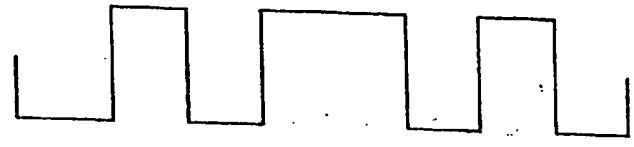

FIG. 15G

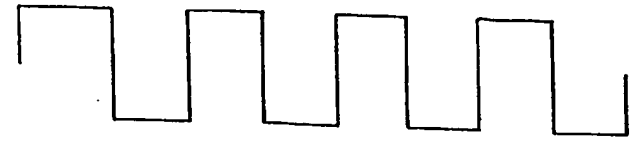

FIG. 15H

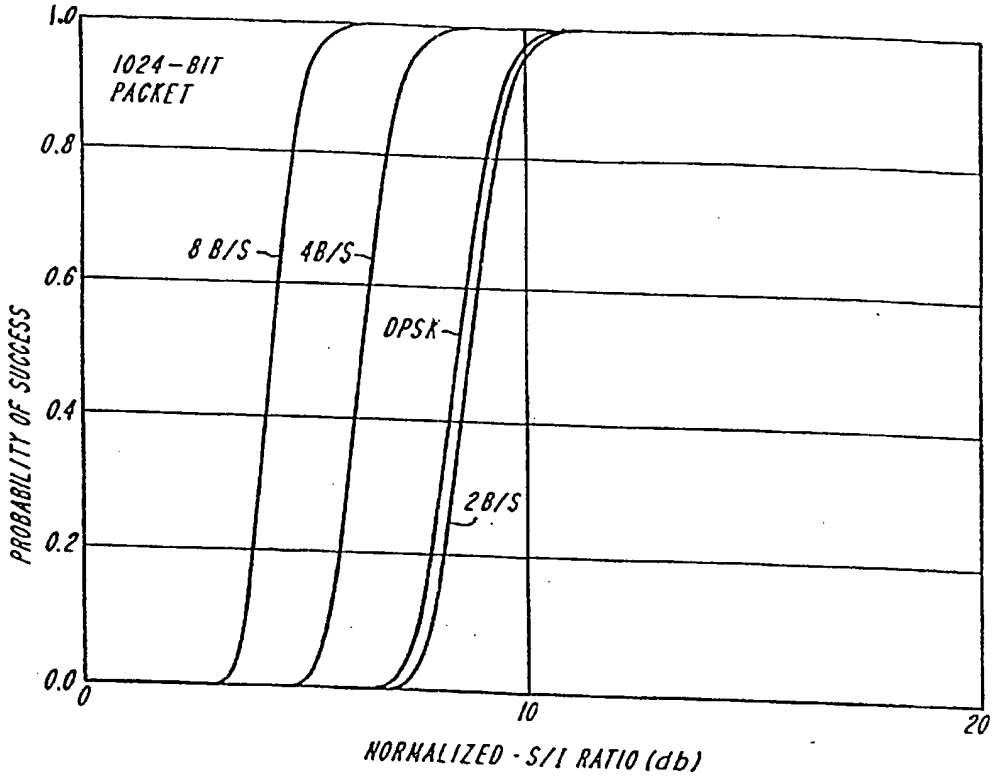
1.0
0.8
0.6
0.4
0.2
0.0
1024-BIT PACKET
8 B/S
4B/S
QPSK
2B/S
PROBABILITY OF SUCCESS
0
10
20
NORMALIZED - S/I RATIO (db)

FIG. 16

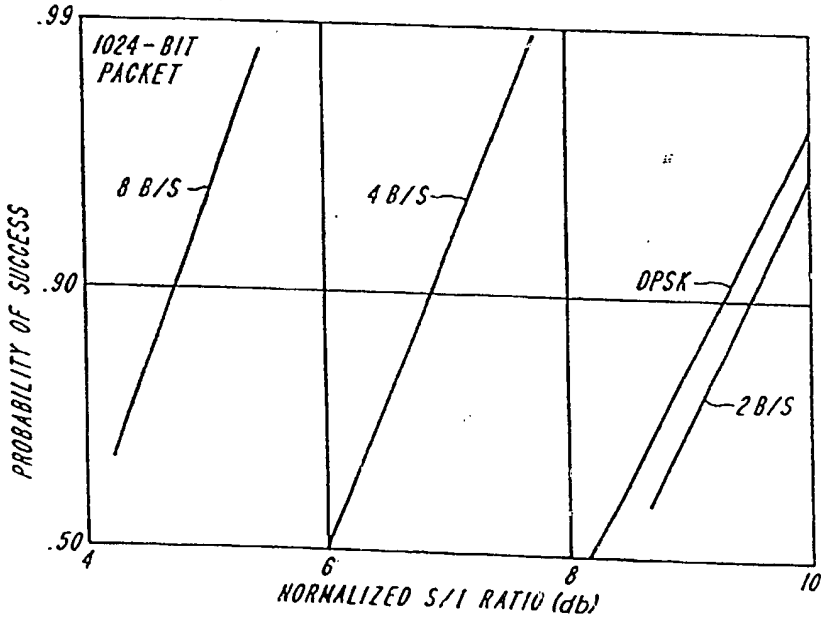
.99
.90
.50
1024-BIT PACKET
8 B/S
4 B/S
QPSK
2B/S
PROBABILITY OF SUCCESS
4
6
8
10
NORMALIZED S/I RATIO (db)

FIG. 17

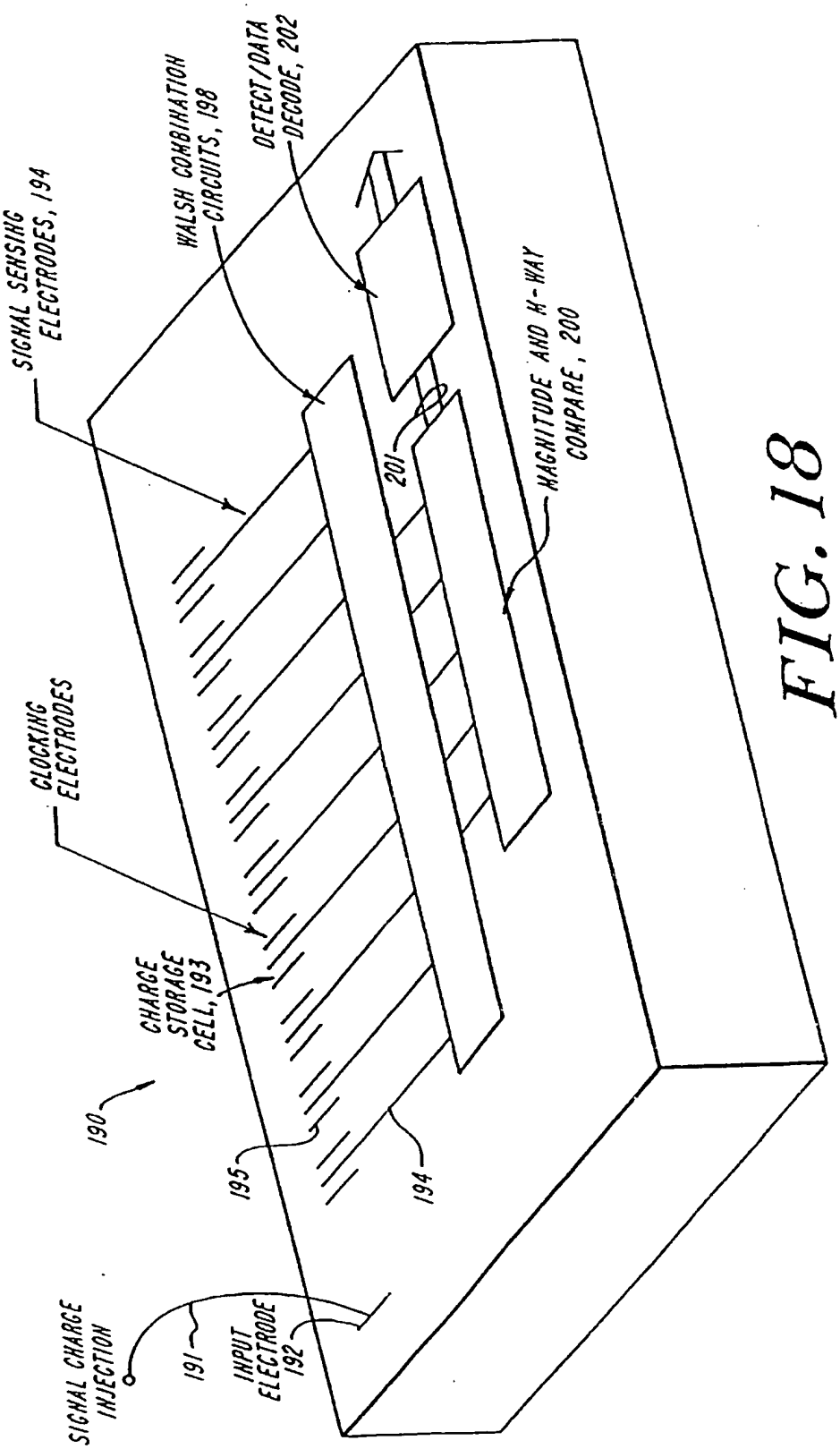
SIGNAL SENSING ELECTRODES, 194
WALSH COMBINATION CIRCUITS, 198
DETECT/DATA DECODE, 202
201
MAGNITUDE AND M-WAY COMPARE, 200
CLOCKING ELECTRODES
CHARGE STORAGE CELL, 193
190
195
194
SIGNAL CHARGE INJECTION
191
INPUT ELECTRODE 192

FIG. 18

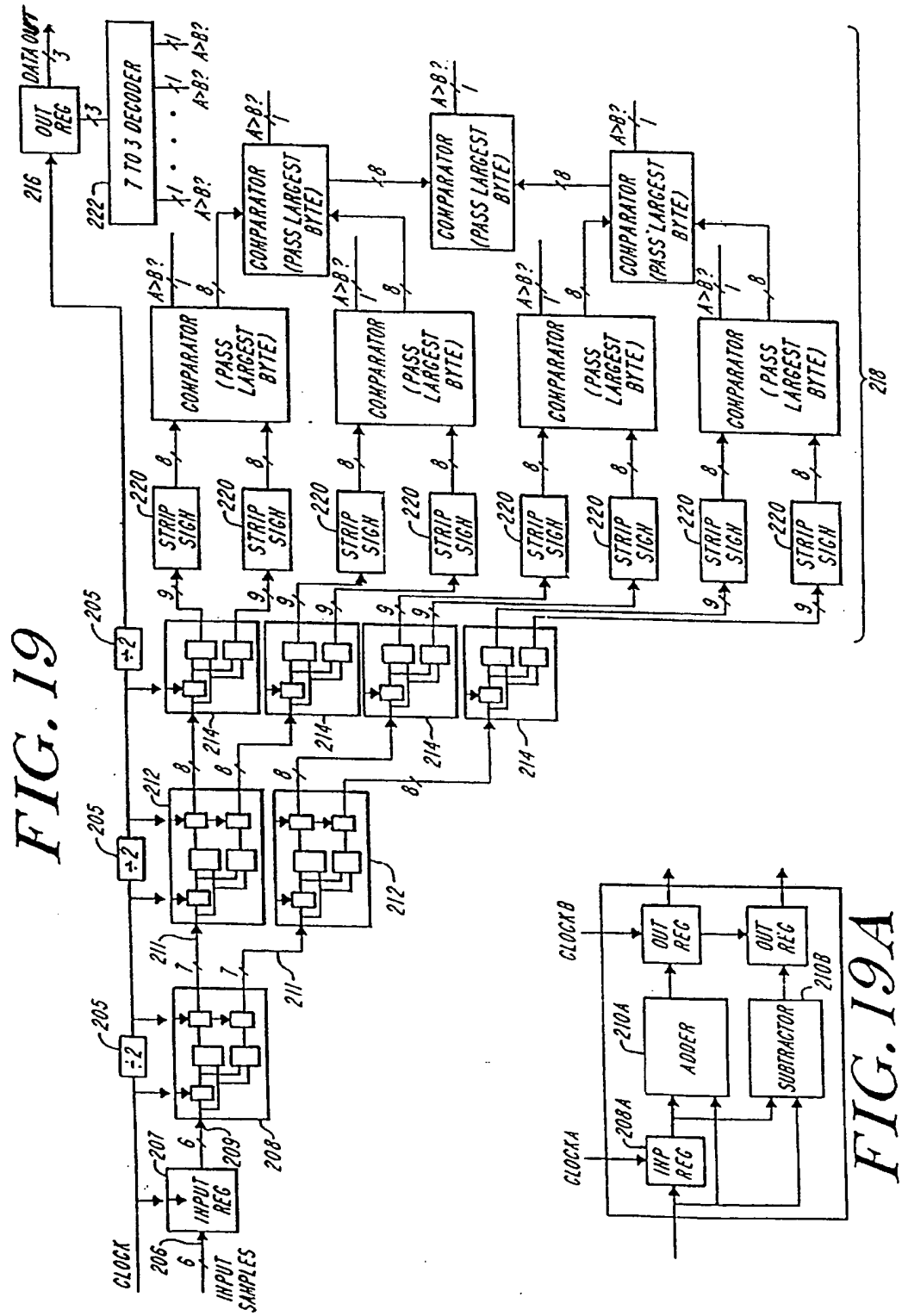

FIG. 19

FIG. 19A

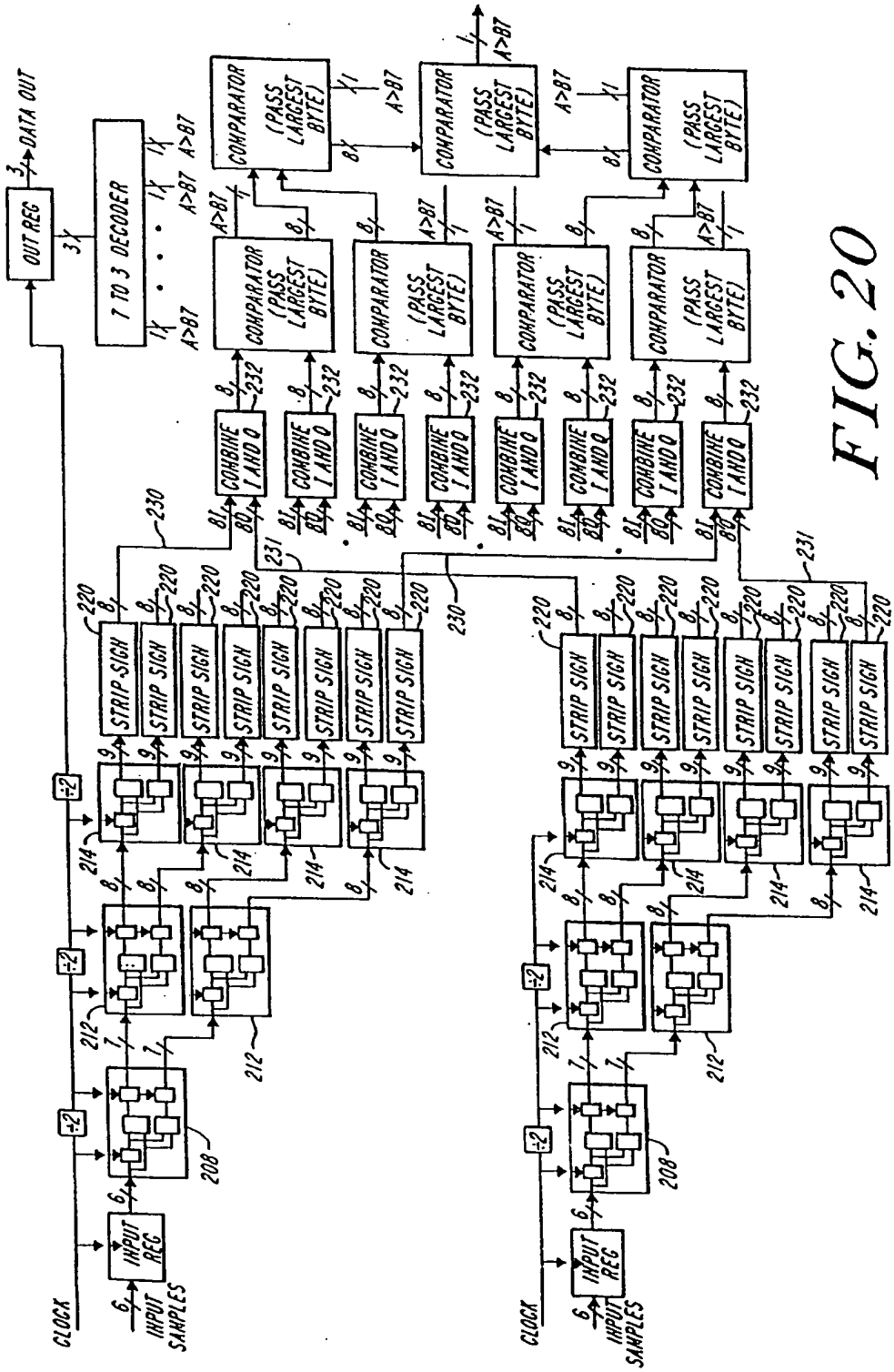
CLOCK
INPUT SAMPLES
INPUT REG
OUT REG
DATA OUT
7 TO 3 DECODER
COMPARATOR (PASS LARGEST BYTE)
COMBINE 1 AND 0
STRIP SIGN
÷2

FIG. 20

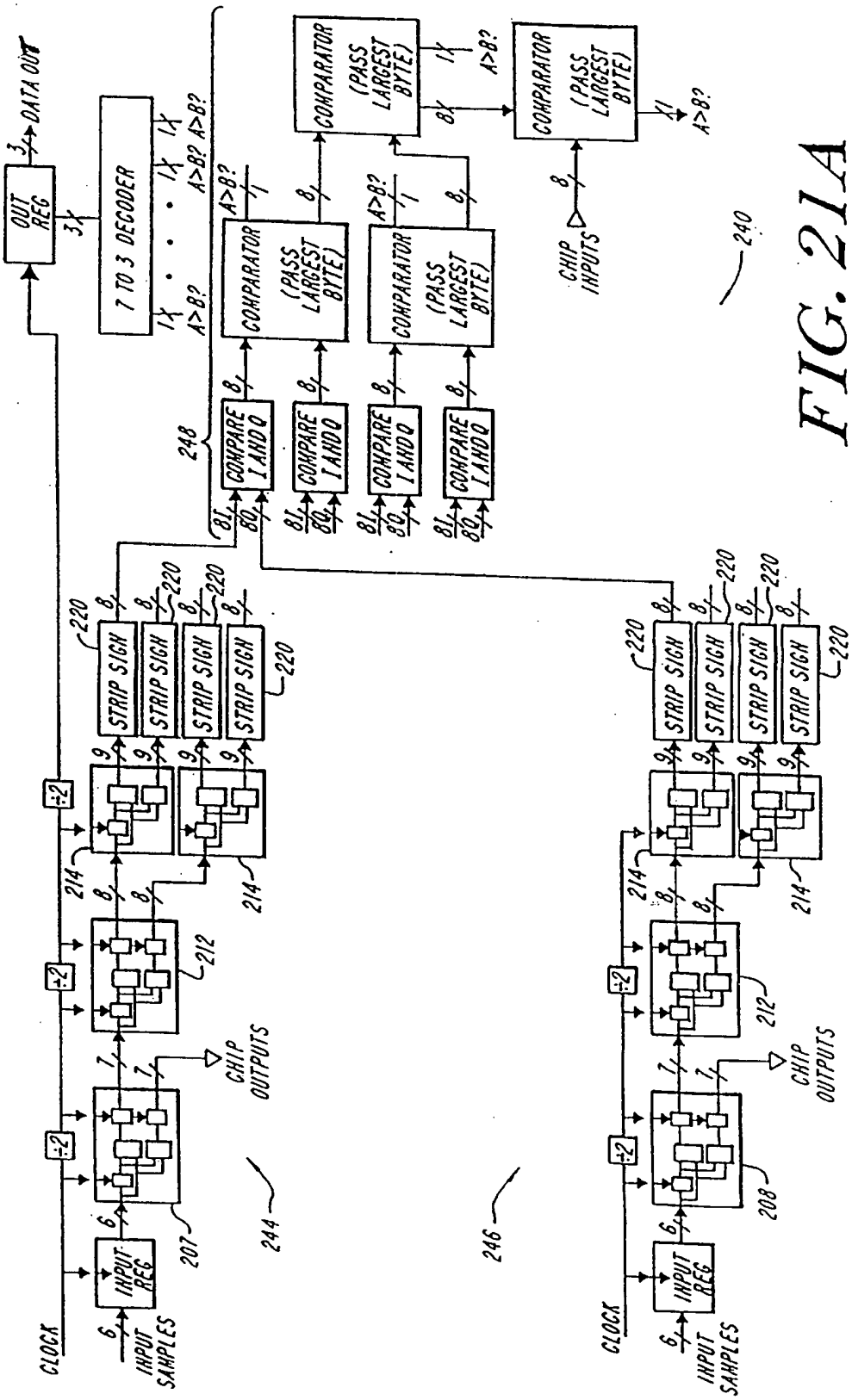
CLOCK
INPUT SAMPLES
INPUT REG
÷2
CHIP OUTPUTS
STRIP SIGN
COMPARE 1 AND 0
COMPARATOR (PASS LARGEST BYTE)
7 TO 3 DECODER
OUT REG
DATA OUT
CHIP INPUTS
A>B?
244
246
240
248
207
208
212
214
220

FIG. 21A

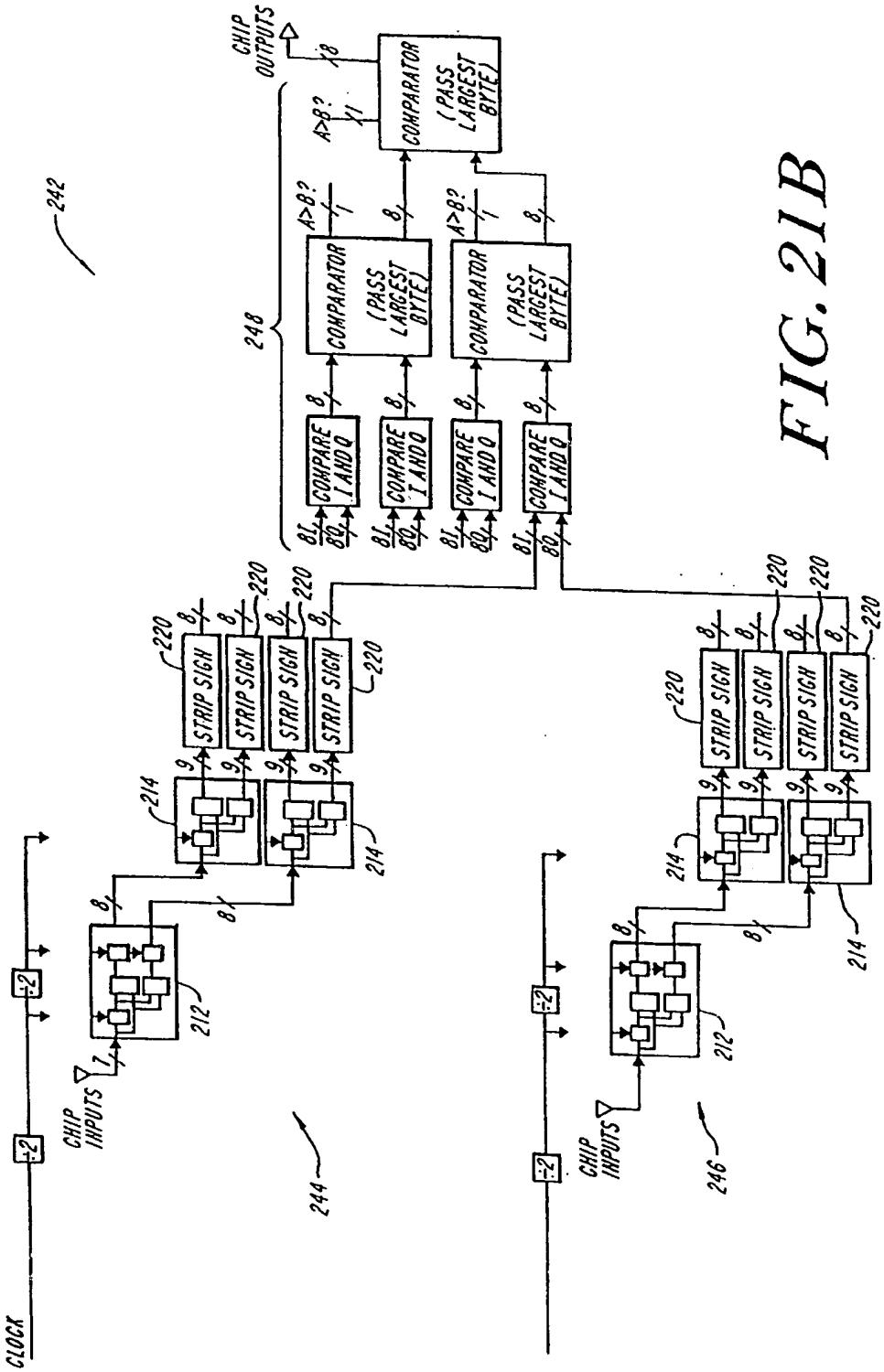
CLOCK
÷2
÷2
CHIP INPUTS
212
214
STRIP SIGN
220
244
246
248
242
COMPARE 1 AND 0
COMPARATOR (PASS LARGEST BYTE)
A>B?
CHIP OUTPUTS

FIG. 21B

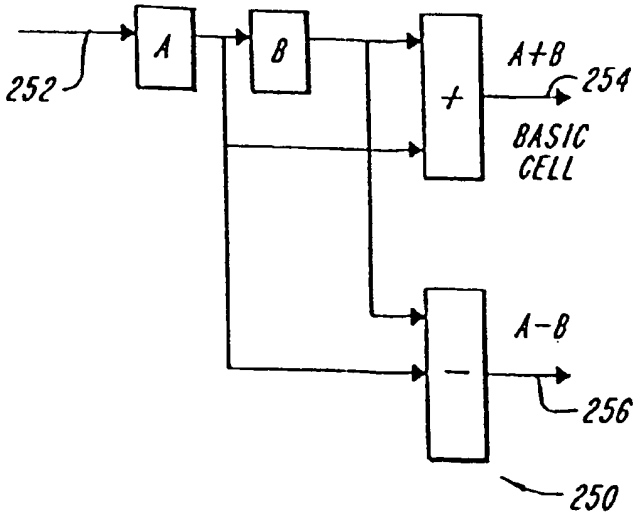
252
A
B
+
A+B
254
BASIC CELL
A-B
−
256
250

FIG. 22

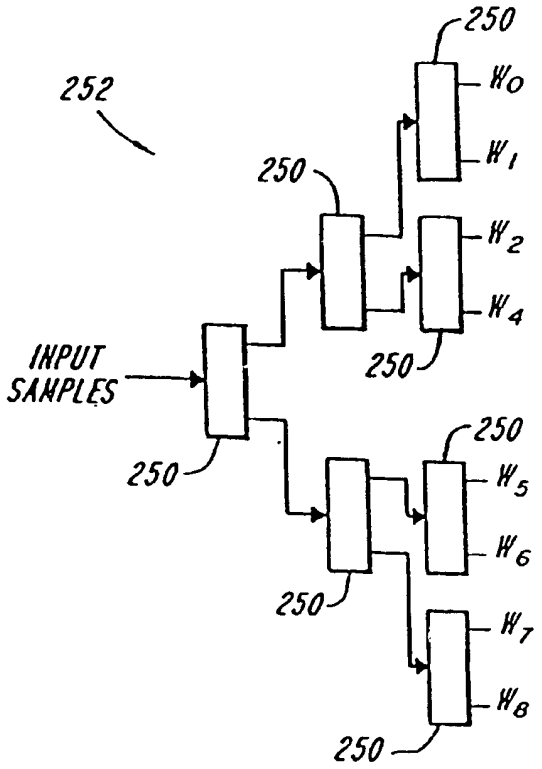
252
250
W_0
W_1
250
W_2
W_4
INPUT SAMPLES
250
250
250
W_5
W_6
250
W_7
W_8
250

FIG. 23

HIGH-DATA-RATE WIRELESS LOCAL-AREA NETWORK

RELATED APPLICATION

This application is a continuation of U.S. Ser. No. 09048,651, filed Mar. 26, 1998 now U.S. Pat. No. 6,075,812 which is a continuation of U.S. Ser. No. 08/369,778, filed Dec. 30, 1994, now U.S. Pat. No. 5,809,060 which issued Sep. 15, 1998, which is a continuation-in-part of U.S. Ser. No. 08/198,138, filed Feb. 17, 1994, now abandoned.

FIELD OF THE INVENTION

This invention relates generally to wireless local-area networks, and more particularly to wireless local-area networks for use in high-data-rate applications subject to multipath interference.

BACKGROUND OF THE INVENTION

Computer communications networks for allowing computers to communicate data to and from other computers have become common. For example, a user of a first computer can send and receive files and real-time data to and from a second computer. A local-area network (LAN) is a computer communications network which provides computer communications among a plurality of computers situated within a common locale. For example, a LAN is typically used to interconnect personal computers or workstations within an office or school building, or to interconnect computers situated in several buildings of a campus or office park. The computers connected to the LAN typically communicate among one another, and usually also communicate with one or more centralized or specialized computers, such as a host computer, with an output device, such as a printer, and with a mass data storage device, such as a file server.

A computer communications network, such as a LAN, employs a transmission medium to communicate data signals among the plurality of data devices in the network. Usually, the transmission medium is a network of wires. Wires can be cumbersome in that they can present routing problems, occupy space, require installation time, and inhibit the mobility of the computers connected to the network.

To overcome the problems associated with using a system of wires as the transmission medium, a plurality of radio transceivers can be used to communicate radio signals for carrying data messages among the computers in the computer communications network. Use of radio transceivers has gained little acceptance so far due to low data transmission rates and/or unreliability. Typically, if the data transmission rate is lowered, the reliability can be improved. Alternatively, high data transmission rates can be achieved, albeit with reduced reliability.

The principle barrier to high data rate communications between computers in a wireless local-area network is an interference phenomenon called "multipath". A radio signal commonly traverses many paths as it travels towards a receiver. Multiple propagation paths can be caused by reflections from surfaces in the environment, for example. Some of these paths are longer than others. Therefore, since each version of the signal travels at the same speed, some versions of the signal will arrive after other versions of the signal. Sometimes the delayed signals will interfere with more prompt signals as the delayed signals arrive at the receiver, causing signal degradation.

Multipath time-delay spread is the time that elapses between the moment that the earliest version of a transmitted signal arrives at a receiver, and the moment that the latest version of the signal arrives at the receiver.

To understand multipath effects and the instant invention, it is helpful to discuss the term "symbol". One or more symbols can be combined to form a message that conveys meaning. Each symbol must be uniquely recognizable, and is selected from a set of possible symbols, referred to as a symbol alphabet. The number of symbols in the symbol alphabet is referred to as the "order" of the symbol alphabet. For example, the letters "a", "b", and "c" are symbols from the English alphabet, where the order of the English alphabet is 26. The numbers "0" and "1" are symbols of the binary number system, which is of order 2.

It is possible to represent a sequence of symbols from a first alphabet with a symbol from a second alphabet, such as representing the binary symbol sequence "**101**" by the symbol "a". This binary symbol sequence consists of three binary symbols. Since each binary symbol can be either one of two possible symbols, in a sequence of three binary symbols, there are eight possible unique binary symbol sequences. Thus, an alphabet of order eight is required to represent the eight possible unique binary symbol sequences of three symbols each. In general, an alphabet of order $M=2^N$ is required to represent the $M=2^N$ possible unique binary symbol sequences of N symbols each.

Just as binary signalling can be referred to as 2-ary signalling, a signalling system that represents three-element binary symbol sequences using a symbol alphabet of order eight is referred to as 8-ary signalling. In the terminology of communications system design, an 8-ary symbolic representation is said to represent each symbol using "3 bits per symbol".

In general, a signaling system that represents an N-element binary symbol sequence using a symbol alphabet of order $M=2^N$ is referred to as M-ary signalling. In M-ary signalling, the equivalent binary data rate R is the symbol rate S multiplied by the number of bits per symbol N, i.e., $R=S*N$. The number of bits per symbol N is $\log_2 M$. Thus, for 8-ary signalling, N=3, and therefore the equivalent binary data rate is three times the symbol rate (assuming no error correction coding and no overhead bits).

In binary signalling, the equivalent binary data rate is equal to the symbol rate, i.e, R=S, because when M=2, the number of bits per symbol N is one. Consequently, "bit" and "symbol" are often used interchangeably in discussions of binary signalling.

In radio communications, a transmitter includes a modulator that provides a transmitted signal representative of information presented to the modulator. Conversely, a receiver includes a demodulator that receives the transmitted signal and ideally provides the original information represented by the transmitted signal. Commonly, the information presented to the modulator includes a plurality of symbols, where each symbol is selected from a finite set of symbols. For each symbol presented to the modulator, the modulator generates a corresponding symbol waveform selected from a set of discrete symbol waveforms, the symbol waveform then being transmitted over a communications channel to be received by at least one receiver.

Each symbol waveform that is transmitted is subject to distortion and noise, thereby making each received symbol waveform differ from the corresponding original transmitted symbol waveform, and become more similar to other symbol waveforms that were not actually transmitted.

Consequently, it is necessary to decide which symbol of the discrete set of known symbols was most likely transmitted. This decision is performed in the demodulator of the receiver, the output of the demodulator being a sequence of symbols, selected from the known set of symbols, that represents the best estimation of the transmitted symbol sequence.

To decide which symbol sequence has been transmitted, for each transmitted symbol, the demodulator processes the corresponding received symbol waveform for a period of time called a coherent integration interval. It is essential that each coherent integration interval be coincident with each received symbol waveform, thereby providing correct synchronization. In the absence of correct synchronization, the symbol content of the received waveform will be misinterpreted.

To further clarify the concept of multipath interference, consider the case of a message transmitted as a binary data modulation waveform, wherein each message symbol consists of a single bit. When the multipath time-delay spread is longer than the duration of a symbol waveform, symbol waveforms of the first version of the received signal overlap non-corresponding symbol waveforms of the excessively delayed versions of the received signal. This phenomena is called intersymbol interference (ISI).

For example, in a typical indoor or campus radio network environment, the time-delay spread can be greater than 500 nanoseconds (ns). Since in binary data modulation, data rate is the multiplicative inverse (reciprocal) of symbol duration, a time delay spread of 500 ns implies that data rates even much less than two million bits per second (Mbps) will result in significant data errors due to intersymbol interference.

In addition to intersymbol interference, some multipath reflections may exhibit time-delay spreads that are less than the duration of a symbol waveform. This form of multipath interference is referred to as intrasymbol interference, and such interference can cause a significant degradation in the amplitude of the total received signal.

In intrasymbol interference, the multipath time-delay spread is shorter than the duration of a symbol waveform. Thus, symbol waveforms of the first received signal version overlap non-corresponding Portions of corresponding symbol waveforms of the delayed versions of the received signal. Consequently, reflected signals of significant amplitude will cause periodic amplitude nulls in the frequency spectrum of the total received signal due to coherent cancellation at particular frequencies. The bandwidth of the amplitude nulls is inversely proportional to the delay of the corresponding signal that is causing the interference. This phenomenon is known as "frequency selective fading", and it substantially impairs the reliability of communication between a transmitter and a receiver.

Overcoming frequency selective fading is commonly accomplished using diversity methods. These methods include spatial diversity, polarization diversity, and frequency diversity. Spatial and polarization diversity require at least two receivers, each having a separate receive antenna, such that the frequency selectivity pattern is different for each antenna.

Frequency diversity receivers can share a single broadband receive antenna, but the transmitted signal is duplicated and is transmitted on at least two carrier signals that are separated by a frequency bandwidth that is larger than the width of a frequency null. A frequency diversity receiver unit consists of multiple receivers, each tuned to a different carrier frequency. The receiver outputs of either method fade independently, and are combined in one of several known ways to take advantage of this. Since this method employs an independent receiver for each diversity channel used, it can be quite costly to implement.

There are known methods for reducing intersymbol interference due to multipath effects while preserving high data rates. A first method employs highly directional line-of-sight microwave links with high antenna gain, since signals having the longest delays often arrive at angles far from the central axis of the microwave antenna. One problem with this method is that to obtain high antenna gain, the antennas must be large, mounted on fixed platforms, and must be carefully pointed. Such antennas are therefore complicated and expensive to install and move. Large antennas are particularly unsuitable for short range indoor or campus environments.

A second method for reducing intersymbol interference due to multipath effects while preserving high data rates is to use echo canceling techniques implemented using adaptive filters. However, the expense and computational requirements of adaptive filters is prohibitive at the high data rates required in the highly dynamic environment of radio communications.

A third method is to channelize the transmitted waveform into multiple channels, each channel being of different carrier frequency and of lower bandwidth (therefore using longer symbol durations) than the single-channel transmitted waveform. Each channel is then received independently. This approach is excessively costly because one independent receiver per channel is required.

A fourth and less conventional approach is to use M-ary orthogonal signalling, with symbols that are $\log_2 M$ times as long as the binary symbols would be. According to the property of orthogonality, the waveform that represents each symbol has no projection on the respective waveform of any other symbol of the symbol alphabet from which the symbols of the message are selected. Consequently, each symbol in the alphabet is more easily distinguished from other symbols in the alphabet than without the orthogonality property.

If the temporal symbol duration of the orthogonal signal is made much longer than the multipath time delay spread, the effect of the multipath can be reduced. For example, one of many approaches includes the use of M-ary frequency shift keying (MFSK) modulation to encode the high-order symbol alphabet into one of M frequencies. Orthogonal signaling would still require a diversity receiver to overcome intrasymbol interference. Furthermore, orthogonal signalling requires excessive bandwidth to implement as compared with a conventional communications channel, and is therefore typically prohibited by government regulation.

All of these approaches for reducing intersymbol interference due to multipath effects while preserving high data rates must, in general, also include means for diversity reception to reduce the intrasymbol interference, and consequently must employ duplicate receivers.

Direct-sequence spread spectrum (DSSS) modulation is a multiplicative modulation technique that can be used for resolving and discriminating against multipath interference. A common but unsatisfactory approach to mitigating multipath effects is to employ direct-sequence spread spectrum modulation in conjunction with binary data modulation, where the direct-sequence spreading function of the DSSS modulation is a pseudonoise (PN) waveform. This approach is unsatisfactory because it cannot provide sufficiently high

data rates to support LAN throughput requirements when sufficient processing gain is used for overcoming multipath effects.

The processing gain of a binary-data-modulated spread spectrum waveform is the ratio of the spreading bandwidth of the DSSS modulation to the data bandwidth. The spreading bandwidth is often limited due to constraints imposed by government regulation or by shortcomings of signal processing technology. Lowering the binary data rate increases processing gain and consequently robustness, but sacrifices rate of data throughput.

The ability to reduce both intersymbol and intrasymbol interference due to multipath effects depends on the processing gain of the spread spectrum waveform and receiver, whereas the ability to resolve adjacent paths is a function only of the spreading bandwidth, not of the symbol rate.

It is known to use Walsh-function waveforms to implement code division multiple access (CDMA). CDMA is used to improve the channel capacity of a spread spectrum system where multiple transmitters share the same frequency spectrum. Walsh-function modulation is used to provide separable signals. It is difficult to ensure this separability because of limited processing gain, and hence precise transmitter power regulation is usually required. Further improvements in gain would be desirable.

Gilhousen, U.S. Pat. No. 5,103,459, specifically teaches a cellular telephone system that employs spread spectrum encoding to discriminate among the signals of multiple users. This capability illustrates a well-known CDMA application of spread spectrum signalling. Reduction of multipath interference is not addressed. In the forward channel, Walsh-function signalling is used for improved CDMA performance, not for data modulation. Furthermore, Walsh-function signalling is not used to increase the CDMA processing gain by extending the symbol duration, but only to provide a better CDMA waveform than pseudo-noise DSSS would alone provide, because the treatment is such that the orthogonality property occurs between multiple users sharing the same frequency band, and not between data symbols. Although Gilhousen '459 discusses the use of Walsh-function data modulation in the reverse channel, Gilhousen '459 clearly states that the purpose of the Walsh-function signalling is to obtain good Gaussian noise performance in a Rayleigh fading multipath channel. Consequently, use of a modulation, such as binary phase shift keying, that requires a coherent phase reference signal for demodulation is precluded. Gilhousen '459 states that differential phase shift keying will not operate well in a Rayleigh fading multipath environment, and some means of orthogonal signalling is required to overcome the lack of a phase reference. Moreover, since the multipath channel discussed in Gilhousen '459 is Rayleigh fading, Gilhousen '459 does not resolve and discriminate against multipath interference. Further, the use in Gilhousen '459 of Walsh-function signalling for data modulation is independent of the use therein of spread spectrum encoding. Gilhousen '459 explicitly states that binary orthogonal signalling also works, since a coherent phase reference would not be required. The receiver described in Gilhousen '459 requires that the entire forward and backward channel be utilized to time-synchronize the mobile units. In fact, a satellite-based timing system is required to keep time aligned between cells. Therefore, the system disclosed by Gilhousen '459 is clearly a time-synchronous CDMA cellular telephone communications system, and is not intended for, or useable as, a high data-rate radio-frequency inter-computer communications system.

Kerr, U.S. Pat. Nos. 4,635,221 and 5,001,723, describes a system that utilizes the bandwidth available in a surface-acoustic-wave convolver, which generally has a much higher processing bandwidth than the bandwidth available for signal transmission. A received signal is multiplexed onto several carrier frequencies, and each is processed independently in the convolver. The convolver is used to simultaneously compare the received signal to M orthogonal reference waveforms, composed of Walsh function and PN-DSSS waveforms. The '723 patent describes a variation that uses orthogonal sinusoids instead of Walsh functions, as taught by the '221 patent. The scope of the teachings of these patents is narrow in that they specifically address a method of demodulating a plurality of signals using a convolver, and do not disclose any means for implementing a high-data-rate wireless local-area-network suited for use in a multipath environment.

Groth, U.S. Pat. No. 4,494,238, discloses use of pseudo-noise direct-sequence spread spectrum across multiple, non-contiguous carrier frequencies that are coherently processed at a receiver. Walsh functions are used in this system to generate signals within the receiver, such signals being used to perform phase computations, but not for signaling over a communications channel corrupted by multipath interference.

McRae et al., U.S. Pat. No. 4,872,182, provides a method for determining a useful frequency band for operating a high frequency radio communications network. Each receiver is identified by its pseudonoise direct-sequence spread spectrum reference code, which implies that spread spectrum encoding is used for CDMA purposes, even though the term "CDMA" is not explicitly mentioned. Walsh-function modulation is used to specify control information for scanning available frequency bands until a useful frequency band is found.

OBJECTS OF THE INVENTION

It is a general object of the present invention to provide a wireless LAN of the type described that overcomes the problems of the prior art.

More specific objects of the present invention include providing a wireless LAN that achieves superior data rates while providing reliable communications.

Another object of the invention is to overcome intersymbol and intrasymbol interference resulting from multipath effects, and to thereby provide a higher data rate with more robust performance than previously possible.

Another object of the invention is to provide a practical means for implementing a high-reliability, high-data-rate, wireless local-area network.

SUMMARY OF THE INVENTION

The invention provides an apparatus and method for providing high data rates in a wireless local-area network data communications environment, even in the presence of multipath interference. To achieve this, the invention combines a higher-order signaling alphabet, such as an orthogonal signal set, with direct-sequence spread-spectrum modulation (DSSS) to provide processing gain for suppressing both intra-symbol and inter-symbol interference due to multipath effects, while also providing the high rates of data throughput required of a wireless LAN. Furthermore, the use of DSSS in this high data rate application reduces intrasymbol interference effects to the extent that the need for diversity methods is significantly diminished.

Use of a higher-order signalling alphabet results in a symbol waveform that is $\log_2 M$ times longer than an equivalent binary signalling waveform, where M is the order of the higher-order signalling alphabet. The longer-duration symbol waveforms of the higher-order signalling alphabet are co-modulated with a DSSS waveform so as to provide increased processing gain for a given data rate, without increasing the spread spectrum transmission bandwidth. The increased processing gain results in robust performance at a data rate that is sufficiently high to provide a practical wireless LAN.

For some applications, the use of a non-orthogonal high-order signalling alphabet results in acceptable performance, as measured by a low bit-error rate for a given signal-to-noise ratio. Examples of non-orthogonal symbol sets include quadrature amplitude modulation (QAW signal constellations, and M-ary phase shift keying sets, when transmitting more than two bits per symbol.

In a preferred embodiment, the higher-order alphabet that is used is mutually orthogonal. The use of M-ary orthogonal signaling to implement the higher-order alphabet is normally prohibited by the narrowband channel allocations available; to convey n bits per symbol, the bandwidth required is M times the symbol rate, where the value of M is 2^n. The fine structure (high frequency components) required to support M orthogonal waveforms, as expressed by the exponential relationship between n and M, leads to exponentially increasing bandwidth requirements. For example, for a given symbol rate, increasing the number of bits transmitted per symbol from 4 to 5 results in a 25% increase in throughput (data rate), but requires a 100% increase in transmitter bandwidth.

An example of an orthogonal signalling set that fits within, i.e., is supported by, the bandwidth of a direct sequence spreading code is the Walsh-function waveform set. As a high-order alphabet, these waveforms can be directly modulated by pseudo-noise spread spectrum modulation, without exceeding the occupied transmit bandwidth required for spread spectrum signalling alone. Since spread spectrum frequency allocations and spread spectrum transceiver equipment are inherently wideband, the Walsh-function waveform set does not require additional bandwidth when used in conjunction with DSSS encoding, even though it requires more bandwidth than the signal to be encoded when only Walsh-function encoding is used.

Consequently, use of the words 'spreading' and 'despreading' are to be interpreted as referring to modulation and removal, respectively, of a DSSS encoding waveform, whether or not there is a change in bandwidth due to the DSSS waveform. In the case of a Walsh-function waveform of a bandwidth that is less than the bandwidth of the DSSS encoding waveform, the term 'spreading' and 'despreading' may be understood in a more conventional sense.

The invention employs a Walsh-function waveform set that includes a plurality of mutually orthogonal binary waveforms which can be synchronously modulated upon a spread spectrum code such that all binary transitions of both the Walsh-function waveforms and the spread spectrum waveforms occur simultaneously with a transition of a common clock signal. The clock signal frequency is selected so as to support the finest possible pulse structure in each Walsh-function and spread spectrum waveform. The finest pulse structure that can occur in a waveform determines the bandwidth of the waveform. Therefore, the clock rate establishes the bandwidth of the waveform. As long as a waveform signal transition occurs at a clock edge, a multiplicative composite of a Walsh-function and spread spectrum waveform will not require additional bandwidth beyond the bandwidth of its two constituent waveforms. Consequently, Walsh-function waveforms having a bandwidth less than or equal to the bandwidth of the DSSS waveform can be used without any increase in bandwidth of the Walsh-function/DSSS composite waveform.

In another preferred embodiment, the orthogonal signal set is supplemented with an antipodal signal set to form a bi-orthogonal signal set, further increasing the data rate achievable at a given DSSS processing gain. Other embodiments include: noncoherent signalling across two symbols, as in differential phase shift keying (PSK), to perform the bi-orthogonal signalling; coherent and noncoherent M-ary phase shift keying, combined with orthogonal signalling within a single symbol; and differentially encoded coherent phase shift keying across two symbols, with orthogonal signalling within a symbol.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood from the following detailed description, in conjunction with the accompanying figures, wherein:

FIG. **1** is a schematic representation of a communications channel affected by multipath interference;

FIG. **2** is a plot of time versus the log of measured impulse response of a typical short range multipath channel exhibiting both intrasymbol and intersymbol interference;

FIG. **3** is a block diagram of a spread spectrum transmitter and time-domain representations of associated waveforms;

FIG. **4** is a block diagram of the correlation process used in a receiver to despread a line-of-sight (LOS) signal encoded by DSSS, and then corrupted by communications channel interference, thermal noise, and multipath effects;

FIGS. **5A**, **5B**, and **5C** are, respectively, a time-domain signal plot of line-of-sight and reflected signals, a block diagram, and a correlation process output plot, together showing a correlation process operating on the sum of the line-of-sight and reflected signals to produce a correlation process output trace;

FIG. **6** is a plot of time versus the log of measured impulse response showing the elimination of the significant intersymbol interference provided by DSSS encoding of each symbol;

FIG. **7** is a chart of LAN types showing rapid synchronization requirements;

FIG. **8** is a block diagram of a spread spectrum transmitter;

FIG. **9** is block diagram of a spread spectrum receiver having a rapid synchronization circuit which provides a timing signal to a correlator demodulator;

FIG. **10** is a schematic of a spread spectrum receiver having a sliding serial correlator for performing synchronization;

FIG. **11** is a diagram of an example of a data packet structure;

FIG. **12** is a schematic diagram of a correlator demodulator that employs bandpass direct-sequence (DS) removal;

FIG. **13** is a schematic diagram of a non-phase-coherent correlator demodulator for orthogonal signalling that employs baseband DS removal and noncoherent DPSK;

FIG. **14** is a schematic diagram of a phase-coherent correlator demodulator for orthogonal signalling that employs baseband DS removal and coherent PSK;

FIGS. 15A–15H are waveform traces showing the first eight Walsh-function waveforms in ascending Walsh order;

FIG. 16 is a plot of the probability of correctly demodulating a 1024-bit data packet versus signal-to-interference ratio for DPSK signaling and orthogonal signalling at various data rates;

FIG. 17 is an enlarged portion of the plot of FIG. 16;

FIG. 18 is an integrated circuit layout diagram of a charge transfer device implementation of a receiver of the invention;

FIG. 19 is a schematic diagram of demodulator chip-circuitry for use with a coherent carrier-phase reference signal;

FIG. 19A is block diagram detailing the add/subtract block of FIG. 19;

FIG. 20 is a schematic diagram of the demodulator chip circuitry for use with a carrier signal of unknown phase, wherein both in-phase and quadrature-phase channels are processed, and wherein the combining circuitry of the demodulator chip is shown schematically;

FIGS. 21A and 21B are schematic diagrams showing a preferred partitioning of the circuitry of FIG. 20 into two chips, or for realizing a cascadeable structure;

FIG. 22 is a schematic diagram of a basic cell for computation of Walsh coefficients; and

FIG. 23 is a schematic diagram of a plurality of the basic cells of FIG. 22 interconnected in a tree architecture, for computation of Walsh coefficients.

DETAILED DESCRIPTION OF THE DRAWINGS

The invention provides an apparatus and method for reducing multipath interference effects, while also providing high data rates in a local-area network data communications environment. The apparatus and method of the invention combines a higher-order signaling alphabet, such as an orthogonal signal set, with direct-sequence spread-spectrum (DSSS) modulation.

As recognized by the invention, an orthogonal signalling set that requires no more bandwidth than the bandwidth of the spreading code of the DSSS modulation is, for example, the set of Walsh-function waveforms. As a high-order alphabet, these waveforms can be combined with a pseud-onoise (PN) direct sequence spread spectrum (DSSS) waveform without increasing the occupied transmit bandwidth beyond the bandwidth required for the spread spectrum signaling alone. The Walsh-function signal set includes binary waveforms which can be synchronously multiplied by the DSSS waveform such that all binary transitions of the Walsh-function waveforms occur at transitions of the same clock signal that generates the DSSS waveform.

The bandwidth of a waveform is determined by the finest possible pulse structure of the waveform. Since each clock transition represents a potential signal transition, the clock rate establishes the finest possible pulse structure of a signal waveform. Any signal transition of the highest bandwidth waveform that occurs at a clock edge will not require additional bandwidth beyond the bandwidth of the clock signal.

There exist other ways to provide an orthogonal signal set for use with spread spectrum techniques. Instead of using a separate multiplicative orthogonal signal set, such as the Walsh-functions, in conjunction with a single pseudo-noise spreading code to implement the signaling, the symbol waveform can be chosen from among a set of nearly orthogonal pseudo-noise (PN) spreading codes, or phase shifts of these spreading codes. Modulations that transmit a variety of shifts of the same code include pulse position modulation (PPM), and cyclic code shift keying, for example, but these time-shift modulations are unsuitable because the demodulation can be ambiguous when subjected to multipath time delays. Modulations that send one of a set of PN spreading waveforms to relay the data also have several problems.

Only PN waveforms that are cyclic, maximal-length sequences without data modulation exhibit the requisite nearly orthogonal cross-correlation properties. Randomly chosen PN waveforms exhibit average cross-correlation values (between different pairs of waveforms) that are equal to the processing gain of the PN waveform. It is difficult to derive a subset of waveforms that have good cross-correlation properties. The number of required waveforms increases exponentially with the number of bits per symbol that must be transmitted. These waveforms, once determined, must be generated with independent PN generators, because each waveform is unrelated to each of the others in structure.

At the receiver, a separate spread spectrum correlator must be provided for each transmitted waveform because the waveforms are generally independent of each other. Each correlator operates upon the received signal, and attempts to provide a level at the output of the correlator representative of the degree of correlation between a received-signal waveform and a reference waveform. Each waveform that can potentially be transmitted will be provided as a reference waveform in one correlator. The data decision as to which waveform was actually transmitted is determined by the correlator with the largest output signal.

By contrast, according to the invention, Walsh-functions do not exhibit these problems. The regular waveform structure of the Walsh-functions allows a set of waveforms of any order to be readily synthesized. In the receiver, the invention exploits a decomposition property of the Walsh-function waveforms that allows a correlator to be constructed from a plurality of identical elements, to be described below. Thus, according to the invention, Walsh-function orthogonal data modulation is the preferred form of data modulation to be used in combination with spread spectrum modulation.

However, any means for providing the correlation against each of a plurality M of Walsh-function waveforms will also suffice. Other examples, such as the fast Walsh transform (also known as the fast Hadamard transform) are equally useful when used in combination with spread spectrum modulation.

An orthogonal signal set is characterized by the property that each waveform has no projection on any other waveform in the set. By contrast, an antipodal signal set is characterized by the property that a waveform can have a negative projection onto another waveform. By combining the two signal sets, a bi-orthogonal signal set is formed, wherein both orthogonal and antipodal signals are possible. As a benefit, bi-orthogonal data modulation provides an extra data bit per symbol, without increasing the transmission bandwidth, or decreasing the processing gain. The accompanying slight increase in required signal-to-noise ratio is insignificant.

A bi-orthogonal signal set can be implemented in the Walsh-function demodulator, as illustrated in the exemplary embodiment of FIG. 14, wherein the positive and negative phase of any of the waveforms can be used as additional potential waveforms in a symbol. Thus, phase shift keying (PSK) can be combined with the orthogonal signalling.

Bi-orthogonal modulation can be processed coherently if the phase of the received signal is tracked.

Alternatively, bi-orthogonal modulation can be processed non-coherently using differential phase shift keying (DPSK) between symbols, as illustrated in the exemplary embodiment shown in FIG. **13**. If non-coherent DPSK is used, after the orthogonal receiver determines which waveform was most likely transmitted for each pair of consecutive symbols, the DPSK receiver determines whether it is likely that there was a phase inversion between the carriers of each pair of symbol waveforms. The next pair of symbols for this operation consists of the second symbol of the previous pair and a new symbol, just as in binary DPSK.

Just as coherent PSK can be used on each symbol if a phase reference is created at the receiver, multiphase phase shift keying can be used with orthogonal signalling to increase data rate. However, the bit error rate performance of this type of modulation degrades rapidly as the order of the signal set increases. Furthermore, multilevel DPSK, such as differential quadrature phase shift keying (DQPSK) can be used, which sacrifices bit error rate performance for improvements in data rate.

Several embodiments of the invention provide robust wireless LAN performance. One such embodiment employs a different PN spreading code for each successive symbol in a sequence of transmitted symbols. Errors due to high cross-correlation sidelobes in multipath between transmitted symbols are thereby randomized.

In a preferred embodiment, to further reduce error rates, error correction coding can also be employed. Error correction coding can be used to compensate for the portion of the error rate due to the high sidelobes that can occur under some multipath delay conditions, as measured at the output of the demodulator.

In other embodiments, the same PN code is repeated every consecutive symbol. Use of repeating PN codes can help to reduce the peak cross-correlation sidelobe levels, whereas changing codes cause some randomization of the levels between symbols.

Another embodiment of the invention uses a pulse-shaping filter on spread spectrum code modulation to reduce the bandwidth required to achieve a given processing gain. It is known in the art that a waveform that is square-shaped in the frequency domain, i.e., having no frequency sidelobes, provides the greatest processing gain. Thus, pulse shaping of the code trades higher time sidelobes for lower frequency sidelobes, i.e., squareness in the frequency domain.

Multipath Environment

Referring to FIG. **1**, it is useful to distinguish two major types of multipath interference. "Near-in" multipath interference is caused by the existence of a reflected version **28** of a line-of-sight (LOS) **26** signal that has travelled only a small distance further than the direct line-of-sight signal **26**, thereby causing coherent cancellation and deep fading of the signal power of the received signal, which is a combination of at least the reflected signal **28** and the LOS signal **26**. This type of reflected signal is delayed with respect to the LOS signal **26** no longer than the duration of one data symbol of the LOS signal **26**, and so the interference resulting therefrom is referred to as "intra-symbol" interference. This type of multipath interference results from a signal travel path that reflects off a surface such that it is incident upon the receiver **22** at a small angle with respect to the LOS signal **26**.

Various frequency components of the LOS signal **26** and the reflected signal **28** destructively interfere at the receiver, resulting in nulls in the received frequency spectrum. For example, if a narrowband signal, i.e, a signal occupying a relatively narrow frequency range (commonly used in traditional communications) is used to modulate a carrier signal of a frequency that falls within a null in the received frequency spectrum, and the narrowband signal traverses both an LOS path and a reflected path to a receiver, the amplitude of the received modulated signal will be substantially diminished. It is even possible that the amplitude of the modulated signal will be diminished to an amplitude less than the amplitude of the noise introduced by the communications channel, resulting in data errors. This effect is known as multipath fading.

For example, where a receiver is disposed at a distance of 200 meters from a transmitter, and a signal reflector is disposed at a perpendicular distance of 45 meters from a line-of-sight path between the receiver and the transmitter, a reflected signal that originates at the transmitter, and is reflected towards the receiver by the reflector traverses an additional 20 m with respect to the distance traversed by a line-of-sight (LOS) signal. Thus, in this example, the reflected signal arrives about 65 nanoseconds (ns) later than the LOS signal. If the reflection is specular, which is often the case, the amplitude of the reflected signal can be nearly equal to the amplitude of the LOS, thereby causing deep multipath fading.

"Far-out" multipath interference occurs when a reflected signal travels a distance sufficiently greater than the distance traversed by the line-of-sight signal so as to cause a delay greater than the duration of one data symbol. The interference that results is called "intersymbol interference" (ISI). The causes of reflection can be similar to the causes of reflection in "near-in" multipath, but the geometry of the transceiver locations with respect to the reflecting surfaces creates an excess reflected path length that can extend beyond the symbol duration before it is sufficiently attenuated below the amplitude of the LOS signal. The invention removes the previously existing limitation that far-out multipath interference imposed on the data rate of binary communications.

When the reflection of the signal corresponding to a first data bit overlays the direct path signal corresponding to a second data bit, intersymbol interference (ISI) results. ISI can cause data recovery errors at the receiver. For example, if the transceivers are separated by 200 meters, and a reflector is disposed at a perpendicular distance of 150 meters from the line-of-sight path and equidistantly with respect to each transceiver, there is a reflected path that is 160 meters longer than the direct path traversed by the line-of-sight (LOS) signal. Thus, the reflected signal arrives at a time that is about 535 ns after the arrival time of the LOS signal. Binary signalling would be limited to much less than 2 Mbps in this operating environment.

FIG. **2** shows a plot of a typical filtered impulse response measurement of a wireless LAN communications channel. Here, T represents the duration of the symbol. The initial (filtered) pulse represents the line-of-sight response to an impulse that is transmitted. All later responses are due to reflections. Both the intrasymbol and intersymbol interference are apparent for this value of T.

Spread Spectrum Performance Advantages

With reference to FIG. **3**, pseudonoise direct-sequence spread spectrum techniques (PN-DSSS) employ a multipli-

cative modulation step that distributes the transmitted signal over a greater range of frequencies (bandwidth) than is normally required to support the data rate. For example, binary data **30** is used to phase-shift-key-modulate a carrier signal **32** in a first modulator **34**. The output **36** of the first modulator **34** has a frequency bandwidth that is on the order of the data rate of the binary data **30**. The sharp signal transition **38** in the modulating data signal **30** causes a phase inversion **39** of the modulated signal **36**. According to Fourier transform theory, the phase inversion **39** introduces high frequency signal components within the signal bandwidth.

The finest pulse structure **40** in the PN-DSSS spreading code **42** is commonly referred to as a chip **40**, to distinguish it from a bit, which refers to the smallest possible pulse of a data signal. The PN-DSSS spreading code **42** phase-shift-key modulates the waveform **36** within a second modulator **44**, resulting in many more phase inversions within each data symbol of an output waveform **45**. The output waveform **45** of the second modulator **44** has a bandwidth that is equal to the bandwidth of the PN-DSSS code. The order of application of the modulations of modulators **34** and **44** can be reversed, and the modulations can also take the form of minimum-shift-keying, or various other continuous-phase-shift-keying waveforms that are known in the art.

Referring to FIG. **4**, within a receiver **46**, the spreading code **42** is removed by a correlation process, such as can be implemented in a matched filtering or serial correlator **48**, using a reference code **49**. The correlation process implemented by the correlator **48** provides a linear decomposition **50** of the individual propagation paths that make up the received signal. The decomposition is inherent in the signal processing and requires no feedback. Therefore, wideband channel dynamics can be handled without computational strain, in contrast with adaptive equalizer systems.

As depicted in FIG. **4**, the correlation process **48** within the receiver **46** performs a cross-correlation of the local reference code **49** and the received signal **47** after it has been corrupted by transmission through a communications channel. The correlation process output **50** is depicted for a range of relative displacements of the received signal with respect to the reference code signal. The spreading code signal **42** is chosen such that the amplitude of its autocorrelation function is nearly zero everywhere except where the signals are aligned. Where the signals align, there occurs a triangular pulse, called a correlation spike **50**, of width $2/T_c$ at its base, where T_c is the chip width.

The peak of the correlation spike **50** occurs at perfect alignment. Recall that each bit of the spreading code is referred to as a chip, to distinguish it from a data bit. Thus, if there are sixteen chips of spreading sequence in a cross-correlation interval, e.g., the duration of a symbol, there are **16** possible ways the spreading code can be aligned with respect to the signal to be correlated, when the chip edges are also aligned. Fractional chip timing shifts account for unknown chip boundary timing. The correlation process determines which of the relative positions results in significant signal energy (correlation spike), the remaining relative positions having negligible signal energy, i.e., no appreciable signal spike.

Referring to FIG. **5**, PN-DSSS spread spectrum modulation of the reflected signal **52** and the LOS signal **54** allows them to be resolved in time at the receiver using the correlation process **56**, thereby eliminating multipath interference. After the correlation process **56**, each signal **52** and **54** is represented by a displaced correlation spike **52***a* and **54***a*, respectively, each spike having an amplitude which represents relative received signal strength. In fact, the output of the correlation process, as the relative code alignment is swept out, approximates the impulse response of the communication channel resolved to the spreading bandwidth, as it is the linear sum of the autocorrelation functions of all of the signal paths.

According to the invention, a benefit of the use of PN-DSSS spread spectrum signaling is the mitigation of severe far-out multipath ISI. In a preferred embodiment, this is achieved by changing the spread spectrum waveform on each data symbol so that the ISI from each data symbol does not correlate with the DS code on any following symbols.

FIG. **6** is a plot of the correlation process output for the channel impulse response of FIG. **2**. The far-out multipath portion of the channel impulse response **58** has been truncated beyond the symbol time because each data symbol is modulated by a different PN-DSSS waveform.

The correlation process can be implemented by using a serial correlator or a matched filter, or an approximation to either. A serial correlator (also called a sliding correlator) tests for signal detection after a period of processing called the detection interval. A detection interval is typically longer than a data symbol because more signal energy is needed to detect a signal than is needed to demodulate the signal to ensure acceptable wireless LAN performance.

The longer detection intervals are achieved by further integrating (either coherently or non-coherently) over multiple coherent-integration intervals, where each coherent-integration interval is of a duration normally associated with a data symbol. After a detection interval, if signal detection is not achieved, the serial correlator slides the reference timing by a fraction of a PN-DSSS code chip. The number of detection intervals that must be checked is the determined by the uncertainty in code timing and the amount of oversampling of the chip timing. For example, if timing is completely unknown and the detection portion of the preamble is a repeated sequence of sixteen chips, with a correlation every half chip for oversampling to prevent straddling loss, then no more than thirty-two detection intervals are required to achieve the proper timing for detecting a received signal. If the detection interval is ten symbols long, the transmitter must send a preamble that is 320 symbols long before sending any data. Furthermore, since the DSSS sequence is repeated within the preamble, and detection can occur on any repetition, after signal detection occurs, frame synchronization must be obtained to determine which symbol is the beginning of the data stream. Since there is sufficient signal-to-noise ratio for detection, frame synchronization can be accomplished using a simple frame sync bit pattern structure that is easily recognized.

It is commonly known that a matched filter synchronizer, or an equivalent device, can test all code timing relationships in a single detection interval, and therefore can serve as a fast synchronizer. The matched filter synchronization will be unambiguous in timing, in contrast with a serial correlator. Various approximations to a full-scale matched filter include a binary-quantized-input matched filter, or a matched filter that includes some non-coherent processing, or a matched filter that performs the full timing search in several steps (but not to the extent of a serial correlator).

The choice of whether to use a correlator or a matched filter for synchronization depends on the application. A correlator is much less expensive and less technology dependent. A matched filter is computationally intensive. A correlator can be used if the application can tolerate long

synchronization overheads, or if there is a means to aid the detection process using a suitable data link protocol.

Local-area Network Channel Access Protocol

A communications-channel access protocol is a set of procedures that enables multiple users to access a common communications channel. For example, in some communications environments, where a plurality of transmitters use the same communications frequency band, a communications-channel access protocol, based upon throughput requirements and communications traffic priorities, requires that each of a plurality of transmitters take turns transmitting over the channel. To send large blocks of data, computer communications protocols often break the data into smaller blocks called packets and send these. The packets are re-assembled at the receiver. Packetizing the data allows multiple users to share the communications channel fairly and efficiently.

FIG. **7** compares six known protocol types with respect to the speed of the synchronizer circuit required. The protocol that is used affects which speed synchronizer is required because synchronization overhead affects average data throughput. For example, signal detection in a serial correlator synchronizer is slow, in general, but its speed can be improved by using prior timing information if such use is supported by the protocol. The timing information can be determined by long-term tracking of timing at coarse resolution to minimize the timing uncertainty on each data packet. Alternatively, the timing information can be determined by central control of timing through broadcast transmissions from a timing hub. This type of communication system will be referred to as "time-slotted" to suggest the synchronous nature of the control information.

If the channel is not time-slotted, but is instead random access, then the length of the data packet used is critical. If the data packets are much longer than the preamble required for serial correlator synchronization, then the preamble will not affect the communications channel throughput efficiency. However, if it is desirable for the duration of the data packet to be short compared to the preamble, then a fast synchronizer must be used to preserve channel efficiency. Short data packets are sometimes required for optimizing traffic flow according to the type of data that is to be transmitted, for re-transmission control, or for operating in burst-interference environments.

It is commonly known that a matched filter synchronizer, or an equivalent device, will test all code timing relationships in a single detection interval, and therefore can serve as a fast synchronizer. It is essential that the synchronizer used is fast enough to obtain the low synchronization overhead required when short data packets are used.

Another approach is a network based on message switching instead of packet switching. In message switching, communications traffic is packetized, but each user of the channel transmits messages, where each message includes a series of packets, and no other user can interrupt a message. The synchronization does not need to re-occur in each packet as it does in packet switching where each consecutive packet can be transmitted by a different user. As seen in the chart of FIG. **7**, only the packet switched, random access protocol that uses short packets requires a fast synchronizer.

If the transmissions are message switched, or if the packets are longer than the clock stability or Doppler shift will allow, then a time-tracking loop must be used to maintain synchronization throughout a transmission. As an example, assume that a data rate of 5 Mbps and a packet length of 200 Kbits are used, resulting in packets of 40 ms duration. If the required time alignment must be held to within 20 ns (which must be substantially less than the duration of a code chip) of the initial synchronization timing, then a net clock offset of 20 ppm is required between the transmitter and receiver. Alternatively, a delay-locked timing control loop can be used to maintain the reference code alignment with the received signal. Alternatively, an automatic frequency control (AFC) loop can be used to lock the clock frequencies.

An embodiment of the transmitter for the wireless LAN communication system of the invention is shown in FIG. **8**. A computer interface **60** provides a stream of binary data which is first divided into a sequence of data words by a symbol grouping module **62**, each data word representing a symbol value. The symbol values may be optionally passed through an encoder **64** for error correction coding. For orthogonal signaling, Reed-Solomon error correction codes may be used with symbols matched to the modulation alphabet. For bi-orthogonal signaling, Reed-Solomon codes can be used exclusively, or a hybrid Reed-Solomon/binary coding technique can be used wherein Reed-Solomon coding is used to correct the orthogonal-demodulation process, and binary correction is used for symbol-to-symbol phase-inversion demodulation. Erasure decoding, whereby potential errors are indicated in the decoder based upon, for example, amplitude information, is an option with either orthogonal or bi-orthogonal signaling. For example, a symbol error that arises during orthogonal demodulation would make suspect the validity of a phase-inversion decision using the corresponding erroneous symbol.

More specifically, error correction coding commonly strives to correct a large number of correctable errors within a group of symbols. The group is called a "coding block". The Reed-Solomon coding block comprises a set of the original data symbols concatenated with some "check" symbols that appear the same as the data symbols but actually contain the coding information. As more check symbols are included with the data, more data symbols which are in error can be corrected. The ratio of data symbols to the total group size is called the "coding" rate. For example, "rate 1/2" coding means there are an equal number of data symbols and check symbols. Rate 1/2 is considered a low rate code. As a result of low-rate coding, the minimum signal-to-noise ratio in a Gaussian noise environment that the demodulation can effectively operate upon is reduced, and tolerance to bursts of errors can be achieved.

The apparatus and method of the present invention can use coding for a somewhat different purpose, and thus an aspect of the present invention is to include a coding approach that is generally considered unsuitable for the more common coding applications, such as for satellite communications or for correcting errors on hard disk drives used in computers. Those applications generally require low rate codes and large coding blocks to achieve the desired performance. In fact, there are integrated circuits available that implement the common coding approaches and they were found to be unsuitable for this application. As a unique problem of the wireless data communications system based on direct sequence and Walsh orthogonal signaling, depending on the direct sequence code being used and the actual multipath delay, there can be an irreducible error rate that results from multipath self-interference. This means that errors appear in the demodulated data even at very high signal to noise ratios.

To solve this problem, a high rate code is used. That is, a small number of check symbols per data block is preferably

employed. This unique way to use coding eliminates the irreducible error rate while maintaining the high throughput requirements of the wireless data communications network. If the more common coding approach were used, the irreducible errors would be eliminated, but at the cost of a severe drop in data throughput, and a severe increase in hardware and software complexity. According to an aspect of the present invention, while such costs are often deemed necessary for other applications, it is not desirable for solving the multipath problem in the wireless data communications network.

The high rate error correcting code may be aided by changing the direct sequence code on each symbol, which randomizes the effect of the multipath on each symbol, even though the multipath is static between symbols. Furthermore, a short coding block is preferably used. The short coding block allows the high rate code to provide robust packet performance even with a small amount of correctibility within each block. There are other reasons that the smaller coding block is desireable: a smaller library of direct sequence codes may be used from which codes are selected for changing on each symbol within a block; less latency occurs between the demodulator and the computer; there are less computational requirements, and less data storage is used while the correction is invoked.

For applications which must be tolerant to bursts of errors, only a large coding block can be used. For random errors, on the other hand, a given code rate, and hence tolerance to some average error rate, may be achieved by different block sizes as long as the ratio of check symbols to block symbols is the same. Because longer code blocks offer somewhat better performance, conventional coding designs normally employ long blocks. The term "short block" as used herein means a block size small enough that a given average random error rate may be tolerated with only the ability to correct a single error. While conventional coding implementations must employ complex, iterative decoding procedures running in sophisticated processors, single-error-correcting codes may be decoded directly using relatively modest digital logic. Thus, the use of a short coding block allows high-data-rate error correction with low delay and simple circuitry.

As a preferred embodiment, the high rate code is a single-error-correcting Reed-Solomon code whereby only one symbol in each coding block may be corrected. Thus a simple implementation of a decoder may be built that uses a simple symbol wide feedback shift register or a look-up table containing the entire decoding operation when the encoded signal is received, as described in greater detail, hereinafter. A coding block that is 15 symbols long with 2 check symbols forms a single-error-correcting Reed-Solomon coding block that is rate 13/15 (also written as RS(15,13)), which can handle symbol-error rates approaching 1/15, and which can be decoded at the receiver within a minimal time period and with a minimum of computational complexity.

The basic RS(15,13) code is used for just the Walsh-Orthogonal part of the signaling (with either coherent or noncoherent demodulation). For Walsh-Bi-Orthogonal signaling (coherent or noncoherent demodulation) it is necessary to provide for correction of the binary element of the data in addition to the Reed Solomon coding. At the symbol signal-to-noise ratios required for orthogonal modulation, errors in the binary portion of the waveform are several orders of magnitude less probable than orthogonal-signaling errors, and hence, can be tolerated. If occasionally a transmitted packet of data is lost due to a random binary bit error, this will occur, on the average, much less frequently than packets being lost due to too many orthogonal-signaling errors (more than a single orthogonal error in a 15-symbol block using RS(15,13)).

The effect, on binary signaling, of having made an orthogonal-signaling error, however, is not negligible because the orthogonal demodulation is used to select the processing channel upon which to perform the binary portion of the demodulation. For coherent bi-orthogonal, for example, the occurence of an error in the orthogonal waveform decision will cause a 50% probability of error for the corresponding binary bit. On the other hand, for noncoherent bi-orthogonal signaling, the occurence of an orthogonal-signaling error will cause a 50% probability of error on the two DPSK bits which use that complex amplitude in forming a DPSK decision. Fortunately, the strong correlation between orthogonal-signaling errors and binary errors makes erasure decoding attractive, and erasure decoding requires fewer check bits than for random error correction.

As a specific case, the preferred coding for Walsh-Bi-Orthogonal signaling with bits per symbol employs a 15-symbol block with 13 5-bit information symbols. The two 5-bit check symbols provide for correction when an arbitrary 4-bit orthogonal demodulation error occurs. After the R-S FEC has located and corrected the 4-bit orthogonal-signaling error, then the location of the suspected pair of DPSK bits, likely to be in error, is known. The binary (fifth) bits for each of the 5-bit check symbols conveys, respectively, parity for the even and odd sets of binary bits demodulated. This means that the adjacent binary DPSK bits are checked by different parity bits which makes parity checking useful for DPSK in which errors are likely to appear in pairs. Because random binary errors can be ignored, it is assumed that a single error can occur in either binary data group (even or odd) and the location of the binary bit that is suspect is known when an orthogonal-signaling error has been made. Hence the pair of parity bits is sufficient to correct the binary data.

Referring again to FIG. **8**, the data modulator **66** translates its input data into corresponding Walsh function symbol waveforms, and an appropriate phase change is then optionally added between symbols. The data modulator **66** translates its input symbol value into corresponding Walsh-function symbol waveforms by selecting from either a stored set of waveforms, or by selecting corresponding logic in a digital waveform generator. For the bi-orthogonal or differentially bi-orthogonal modulation, the phase inversion control is accomplished by either complementing or not complementing the binary Walsh-function output so as to increase the information content of the symbols, thereby increasing the data rate. An exclusive OR logic gate **72** then combines the resultant waveform with a PN-DSSS waveform **69** generated by a direct sequence pseudonoise generator **70**. The output of the logic gate **72** drives an RF modulator **74** that provides a transmit signal **76**, which is then amplified by an RF amplifier **78** for broadcast over an antenna **80** as packets of data.

The order of application of the modulations provided by the modules **70**, **72**, and **74** are unimportant, and can therefore be reversed. Also, the RF modulator **74** can be implemented in stages, for example, by first employing intermediate frequency modulation, then employing modulation with a final transmitted frequency, with associated filtering.

The data modulator **66** can incorporate any phase shift modulation, in addition to the selection of the Walsh func-

tion. Coherent M-ary PSK, or non-coherent differential phase shifts between symbols, such as DPSK, DQPSK, or differential M-ary PSK, can be used to increase data rate when signal-to-noise ratio is sufficiently high. Appropriate error correction encoding can be used in conjunction with these modulation schemes.

With reference to FIG. **9**, in one embodiment of the invention, a receiver **84** includes a rapid synchronizer **82**. The output of the rapid synchronizer **82** controls the timing of the combination Walsh-function and PN correlator **86** and the PN reference generator **83**. Various implementations of a Walsh-function/direct sequence correlator, such as the Walsh-function/pseudonoise correlator **86** of FIGS. **9** and **10** are provided in FIGS. **12**, **13**, and **14**. Schemes for fast synchronization are well-known in the art, and can be used in a variety of forms with this invention. One example is a matched filter. Another example is an aided-acquisition correlator. The rapid synchronizer **82** must include a detection circuit with a detection threshold level. The threshold level may be fixed or it may be determined as a function of received signal level.

The correlator **86** drives a demodulator **88** that performs a maximum likelihood decision, or an approximation thereof. The correlator **86** has a plurality M of outputs, the number M of outputs being equal to the order M of the M-ary signal **85** to be demodulated. The particular output of the M outputs having the largest magnitude will most likely correspond to the reference waveform that matches the waveform that was transmitted. Accordingly, the M outputs of the correlator **86** drive the demodulator **88**, which selects the largest magnitude output from among all the correlator **86** outputs.

Any phase shift data modulation that is used in addition to orthogonal modulation can be ideally demodulated by correlating against all possible waveforms in the demodulator **88**. Alternatively, phase shift keying (coherent or noncoherent, and within a symbol or between symbols) can be demodulated separately by operating the demodulator **88** only on the selected orthogonal values resulting in insignificant loss in performance.

In an exemplary embodiment, for DPSK combined with M-ary orthogonal signalling, the M-ary orthogonal waveforms in each symbol pair are first demodulated. The outputs of the correlators that contained the largest outputs on successive symbols would then be used in the DPSK demodulation. In another exemplary embodiment, for coherent PSK combined with M-ary orthogonal signalling, the M-ary orthogonal waveforms in each symbol are first demodulated. The output of the correlator that contained the largest output for each symbol would then be compared to a phase reference in the PSK demodulator.

In the demodulator **88**, after demodulation is performed, each demodulated symbol is then decoded for errors, if error correction coding was employed in the transmitter. The decoded symbols **89** are then concatenated within the data interface **92** to form a binary data stream to be received by a computer.

Note that no delay-locked timing control loop is included, because it is assumed that the packets are short enough to require rapid synchronization. However, a delay-locked loop or an AFC loop can be included if the packets are nevertheless too long for the timing drift specification, or if a variable length packet is desired.

With reference to FIG. **10**, an embodiment of a receiver of the invention is shown that uses correlator synchronization, and includes an optional delay-locked time-tracking control loop **90**. Any of the Walsh waveforms can be used as a synchronization signal transmitted at the start of a packet. As an illustrative example, the lowest order waveform W_0 will be used. In this case, the correlator **86** performs a serial correlator search for the PN code timing,using timing information as an input from aiming control module **87**. The output signal W_0 is detected by a comparator **93**, which can be analog or digital, depending upon the implementation technology of the correlator **86**. The output signal of the comparator **93** is received by a synchronization detector **95**. The synchronization detector **95** then prevents further searching for a signal and enables the demodulation process.

In an exemplary embodiment, the second input **94** to the comparator **93** is determined by the threshold estimation module **98** that sums the respective magnitudes of the outputs of one or more of the other channels **96**. Since these channels **96** are performing orthogonal correlation with respect to the synchronization signal that is transmitted, the channels **96** provide a measure of the noise and interference power in the receiver. In the absence of noise and interference, only one of the channels **96** would be active. However, some degree of noise and interference is inevitable, and therefore each of the channels **96** is active to some extent. Combining a number of these channels **96** allows noncoherent averaging of the noise and interference power of the received signal, thereby providing a detection threshold level that adapts to maintain a nearly constant false alarm rate, where a false alarm is an erroneous interpretation of noise or interference as a true correlation signal. Using simultaneous correlations in orthogonal channels to establish the detection threshold level is superior to methods which average the level of a single correlator over a period that straddles multiple output samples because such methods experience transient response problems.

The demodulator **88** of FIG. **10** is the same as the demodulator shown in FIG. **9**. Note that the optional time-tracking function **90**, used to maintain synchronization during long packets, is explicitly indicated in FIG. **10**, whereas the time-tracking function is implicit in FIG. **9**. Methods for implementing the time tracking module **90** are well-known and include early/late correlation and time dither, and also include APC if the source of timing drift is clock offset or Doppler.

An example of a data packet structure **100** that can be used with the invention is shown in FIG. **11**. The data packet structure **100** includes a header portion **101**, a data portion **102**, and a trailer portion **103**. The header portion **101** includes a preamble **104**, a source address **106**, a destination address **108**, and a packet length **110**. The preamble includes the synchronization signal, and optionally includes signals that the receiver can use to verify that a detection event occurred. The length of the preamble **104** is determined by the type of synchronization used. The preamble **104** can also be followed by other control information, such as error correction type or error checking on the control information itself. The body of the packet holds the data **102**. The trailer **103** includes a cyclic redundancy check code **112** for final error detection. The trailer can also include acknowledgment information **114** regarding the successful or unsuccessful receipt of previous packets; this is known as "piggybacked" acknowledgements.

FIGS. **12**, **13**, and **14** show details of the combined Walsh-function and PN correlator block **86**, and the data demodulator block **88** of FIGS. **9** and **10**. For purpose of illustration only, these examples will use an 8-ary Walsh modulation to provide 3 bits per symbol. However, it should be recognized that the same circuits can be applied to

orthogonal signaling of an arbitrary number of bits per symbol, including binary orthogonal signaling.

Pseudonoise (PN) removal can be performed directly on an intermediate frequency, or on the transmission frequency, by at least one mixer **115** and at least one bandpass filter **116**, as shown in FIG. **12**. If the Walsh-function coding does not occupy the full spread spectrum bandwidth (i.e., if there is more than one PN chip per Walsh-function clock cycle), then the bandpass filter **116** can filter to the Walsh-function bandwidth, resulting in a partial correlation. In this case, the bandpass filter **116**, which can be implemented as a surface acoustic wave (SAW) filter, provides a square-shaped impulse response that filters the input waveform so that it falls within the bandwidth of the Walsh-function modulation. This filtered signal **117** is then split and sampled in I and Q channels by respective mixers **118**, low pass filters **120**, and A/D converters **122** thereby forming a complex representation of the signal **117**, the I channel representing the real component, and the Q channel representing the imaginary component of the signal **117**. The output of the A/D converters **122** is received by the Walsh-function demodulators **124** that correlate the signals with a reference Walsh functions. The outputs of the correlators **124** are envelope demodulated in a combining circuit **126** that provides an envelope output for each set of the eight sets of complex (I and Q) channels for the 8-ary modulation. The eight envelope outputs are compared in a 8-way comparator **130** to provide a largest magnitude index indicating which complex correlator **124** yielded an envelope output having the largest magnitude. The largest magnitude index indicates the most likely data symbol transmitted, as determined by the linear correlation process performed in the correlators **124**. The data decoder **132** receives the largest magnitude index and the eight envelope outputs, and performs either a direct decoding to a binary stream of the selected Walsh-function correlator envelope output, or performs an optional Reed-Solomon, or hybrid Reed-Solomon and binary code error decoding if bi-orthogonal signalling is also used.

FIG. **13** shows and exemplary embodiment wherein PN removal is performed after analog-to-digital conversion, and immediately prior to performing Walsh-function correlation. It is also possible to perform PN removal at baseband using an analog multiplication prior to A/D conversion (not shown). The demodulator can be the same as the demodulator **130**, **132** used FIG. **12**, or DPSK can optionally be added between symbols. This form of signalling is called the non-coherent bi-orthogonal signalling, because DPSK is used.

To perform the DPSK demodulation, the output **152** of the 8-way magnitude comparison module **150**, which module determines the largest correlator output, is used in selector **146** to multiplex to its output, from among the **8** complex amplitudes **145**, the complex amplitude **147** of the largest signal, which complex amplitude **147** is to be used in the DPSK demodulation.

The DPSK decision is made using the selected outputs of two successive symbols in the complex multiplier **158** by using a symbol delay **154**, taking the inner product of the largest amplitude correlator outputs and deciding the sign of the result. Independently, the index of the largest of each symbol is saved in a symbol delay module **156** as the correct value of the Walsh-function signaling. The data decoder **160** receives the Walsh demodulation result from the symbol delay module **156** and the DPSK demodulation result from the complex multiplier **158**. These results are combined in the data decoder **160** by concatenating the single-bit DPSK answer with the 3-bit Walsh-correlator answer to obtain a 4-bit output (16-ary alphabet) on each symbol. Optionally, the data decoder **160** applies an error correction algorithm. The data decoder **160** then converts each resulting symbol into an equivalent binary data sequence for processing by a computer (not shown). The data decoder **160** serves to invert the operations performed by modules **62**, **64**, and **66** in FIG. **8**. Note that symbol delay **156** is optional in accordance with which particular symbol aligns with the transmitted DPSK modulation. With symbol delay module **156** in place, the DPSK result aligns in the data decoder **160** with the Walsh-function symbol that was transmitted during the leading symbol of the DPSK symbol pair.

FIG. **14** shows a single channel demodulator for use with a coherent phase reference signal **164**. An IF signal **166** is filtered by a bandpass filter **168**. The filtered IF signal is multiplied by the coherent phase reference signal **164**, which is provided by a carrier recovery loop (not shown). The resulting signal is low pass filtered by a low pass filter **170**, and is then converted to a digital signal by an analog-to-digital converter **172**. The resulting digital signal is despread by a PN correlator **176** using the PN reference code **174**, and the resulting despread signal is then Walsh-function demodulated in a Walsh correlator **178**. Any of the above described techniques for PN removal and Walsh-function demodulation can be applied, and can be applied in any order. If the PN spreading code is a higher rate modulation than the Walsh modulation, then the despread PN can be collapsed to the Walsh bandwidth in the PN correlator **176**. Because the phase reference signal **164** is used, only a single channel (channel I) is required in this correlator. A sign stripping module **180** strips the sign bit from the digital signal provided by the walsh correlator **178**, and an 8-way compare module **182** determines which correlator output of the correlator **178** is the largest. Since the phase reference signal **164** preserves coherence, optional PSK modulation can be used to provide coherent bi-orthogonal signalling. Demodulation requires that the sign bit of the largest value be selected in the sign register **184**. A data decoder **186** optionally performs error detection and correction, and disassembles the symbol groups of the signal provided by the 8-way compare module **182** into a binary data stream for processing by a computer (not shown).

Walsh-Function Signaling

The first eight Walsh functions are shown in FIGS. **15A–15H**. The lowest order Walsh function is shown in FIG. **15A**, and the other Walsh functions are shown in ascending order in FIGS. **15B–15H**. The lowest order function is referred to as W_0. Since in a communications environment the Walsh functions are a function of time, the Walsh functions may also be represented as W(n,t) or WAL(n,t), where n is the order of the particular Walsh function, and t represents time.

The Walsh functions are digital waveforms each being mutually orthogonal with respect another Walsh waveform of different order when multiplied therewith, i.e., the integral of the product of any two Walsh functions of different order being equal to zero. The order of each Walsh function is equal to the number of binary transitions exhibited by the function. For example, WAL(0,t) does not have a binary transition, whereas WAL(2,t) has two binary transitions. Equivalently, the Walsh function waveforms can be viewed as having one or more binary states over the duration of the waveform, wherein a binary state can be of a duration no greater than a minimum duration, called a Walsh chip.

For each symbol of a message, one of these digital waveforms can be logically combined by an exclusive-or

logic gate with a direct-sequence spread spectrum code to create another digital waveform that can be used to phase modulate a carrier that has been modulated by the message.

FIG. **16** shows four probability curves. A curve denoted by DPSK shows the probability of correctly demodulating a 1024-bit packet of data using DPSK spread-spectrum signaling as a function of normalized signal-to-interference (S/I) in decibels (db). Three additional curves, denoted by the data rates (in bits per symbol) 8 b/s, 4 b/s, and 2 b/s, show the probability of correctly demodulating a 1024-bit packet of data using M-ary orthogonal signalling with 8, 4, and 2 bits per symbol, respectively. It must be stressed that M-ary orthogonal signaling is a form of coding; if the DPSK modulation were combined with coding, it would also shift to a lower required signal-to-interference ratio.

FIG. **17** shows the same curves on an expanded scale. Note that the use of 4-ary orthogonal (2 bits/symbol) is substantially equivalent to DPSK, and that a higher signaling alphabet (4 b/s or 8 b/s) significantly improves performance. For an uncoded link, the above curves imply that, for a given bandwidth, the S/I ratio that can be tolerated at the receiver by combining M-ary (M>2) orthogonal signaling with PN-DSSS spread spectrum is larger than the S/I ratio that can be tolerated by combining PN-DSSS spread spectrum and either binary (M=2) signalling or DPSK. Conversely, for example, a transmission using 4 bits/symbol and a PN-DSSS bandwidth of 80 Mhz can tolerate as much interference at the receiver as a transmission using DPSK and a direct-sequence bandwidth of about 130 Mhz!

A rotation of the PN-DSSS code, known as cyclic code-shift keying (CCSK), provides an orthogonal set with some of the advantages of using the Walsh functions, such as the property that the bandwidth required for orthogonal signaling can equal the direct-sequence bandwidth, without further expansion of the signal bandwidth over that of the PN-DSSS code. Use of CCSK results in a correlator output waveform that is pulse-position modulated (PPM). However, in a multipath environment, the PPM-like behavior of CCSK can be problematic because an important feature of the signal, the delay discriminant used for demodulation, can be incorrectly interpreted as multipath. Thus, the use of CCSK is not preferable to the use of Walsh functions in a multipath environment.

If the bandwidth expansion due to the orthogonal signaling is much smaller than the direct-sequence spreading, then any orthogonal set can be used; in this case a convenient choice is a set of tones (i.e., M-ary PSK) which is demodulated using a fast Fourier Transform (FFT) technique after the spreading code is stripped off. However, when the spreading due to the orthogonal signaling approaches that due to the DSSS modulation, the actual transmission bandwidth depends upon both the direct sequence and orthogonal modulation since the pair of modulations cannot be synchronously superimposed in any way because they are drastically dissimilar modulations.

Even though both CCSK and Walsh functions have the property that the bandwidth required for orthogonal signaling can equal the direct-sequence bandwidth, without further expansion of the signal bandwidth over that of the PN-DSSS, CCSK cannot be used effectively in a multipath environment. Thus, for the purpose of limiting bandwidth and enhancing performance in a multipath environment, the Walsh functions are preferable to CCSK.

Walsh Function Correlation Processor

For this discussion, assume a received signal has been modulated using both PN-DSSS and Walsh functions. Also assume that, in the receiver, the reference PN-DSSS code for demodulating the received signal is properly aligned with the received signal, where synchronization is achieved by using, for example, a matched filter or a time-sliding serial correlator. Further, assume that the received signal and the local reference signal are multiplied together to form a despread signal, and that the despread signal is then low-pass filtered to facilitate processing the highest-order Walsh function. (For example, the highest-order Walsh function can have a bandwidth that only includes frequencies that are less than the DSSS chip rate.) The despreading operation has the effect of removing the PN-DSSS code, leaving only the Walsh function modulation.

The discussion below considers in-phase baseband processing. In an actual implementation, since carrier phase is usually unknown, the signal is converted to in-phase and quadrature channels, and the in-phase processing described below is performed in each channel, followed by envelope combining of the corresponding amplitudes before data decision.

One way to obtain the required correlations in the Walsh function correlation processor (e.g., modules 86, 124, 144, 178) is to implement a fully parallel fast Walsh transform. This approach becomes attractive only as the order of the Walsh functions becomes large. A preferred method for executing a fast Walsh transform is to exploit the mathematical structure of the Walsh functions by computing the Walsh function coefficients using a plurality of basic cells, shown in FIG. **22**, interconnected as a tree structure having successive stages, as shown in FIG. **23**. The clock rate of each successive stage is reduced by half with respect to the previous stage, and each successive stage has twice the number of cells, thereby keeping the computation rate per stage the same at each stage. The power consumed per stage, mostly dependent on computation rate, is therefore also nearly constant. Furthermore, the number of computation elements is far fewer than the number required in the fully parallel fast Walsh transform.

The parallel fast Walsh transform requires M(log M) computation elements per M-ary output. By contrast, the tree structure shown in FIG. **23** uses 2(M−1) computation elements per M-ary output. Therefore, at larger values of M, the tree structure of FIG. **23** is superior to the parallel architecture (not shown) for calculating the Walsh transform, because the number of computation elements per M-ary output is significantly less in the case of the tree structure. Both structures perform the same number of computations per symbol. The tree structure provides an tradeoff that is advantageous when implementing it as an integrated circuit, in that quantity of hardware can be traded for hardware operation rate.

Referring to FIG. **22**, a basic cell **250** accepts input samples serially at input **252** at a rate $f_{in}/2$, and generates two output samples in parallel at outputs **254** and **256** at a rate $f_{in}/2$. Thus, a serial pair of input samples forms a parallel pair of output samples. One output sample of the output pair is the sum of a current pair of serial input samples, and the other sample of the output pair is the difference of these two input samples.

FIG. **23** shows a tree **252** of basic cells **250** for decoding the first eight Walsh functions W_0–W_8. Note that through the application of arithmetic sums and differences, each path through the tree represents a multiplication of the input sequence by a specific combination of (binary) square-wave functions and summing the result. In fact, the specific square-wave function for each path is a product of Radema-

cher functions, whose products are known to generate the Walsh functions.

Also note that the tree structure naturally conserves power because each successive stage includes twice the number of elements as the previous stage, but runs at only half the clock rate of the previous stage. Further, layout of the design on an integrated circuit is simplified, because the higher fanout signal distributions operate at proportionally lower rates. Therefore, slower circuits are connected by longer signal routes, as is desirable in an integrated circuit.

The Walsh function correlation processor can be implemented using a field programmable gate array, although the detailed implementation technique is not relevant. Field programmable gate array implementations are facilitated by the tree structure because the higher fanout routes of such an implementation, being longer, can operate more slowly. Alternatively, the processor can be implemented entirely in software executed by a digital signal processing microprocessor. For high bandwidths, the processor can be efficiently implemented using a charge-transfer device (CTD).

Charge-Transfer Device Implementation

Charge-transfer devices (CTD) include charge-coupled devices (CCD), acoustic-charge-transfer (ACT) devices, and bucket-brigade devices (BBD). Each of these technologies represent signals as electronic charge, and process the signals by manipulating electronic charge. CTD technologies can perform both synchronization and demodulation. A CTD can take discrete-time analog samples at its input, perform all the signal processing, and provide the resulting digital data decisions at its output. Since the CTD input is a capacitive storage cell, the analog signal is inherently sampled as the CTD input is clocked. This operation is similar to the sampling capacitor in a sample and hold circuit.

Alternatively, a digital approach requires high speed D/A converters that are costly. By contrast, the input linearity of a CTD supports far more processing gain than is needed for this application, at sampling rates of 50 Msps for CCD devices to 360 Msps for ACT devices. These sampling rates include a factor-of-two oversampling, relative to the signal bandwidth, to prevent excessive straddling loss. Higher sampling rates are possible by operating two devices in parallel and staggering the clocks. The signal can be processed with analog precision against the binary digital reference signal.

A Walsh demodulator can be configured using a CTD **190**, as shown schematically in an exemplary embodiment in FIG. **18**. The electrical input to a CCD **190** is connected to signal charge injection wire **191** which is bonded to the surface of the substrate at input electrode **192**. A clock signal on the clocking electrodes **195** transfers the sampled charge packet serially along the row of charge storage cells **193**. After each clock period, during which period, each charge storage cell receives the charge packet previously stored in the charge storage cell to its left, the signal sensing electrodes **194** read the level of charge stored in each cell.

Alternatively, in an ACT, signal samples are handled similarly, but the clocking electrodes of the CCD are replaced by the electric potential of a traveling surface acoustic wave. In a BBD, the clocking of signal charge is effected via clocked pass transistors, but the signal treatment is analogous.

A Walsh demodulator requires sample delays for providing storage of waveform samples, as is provided in the charge storage cell **193** that is within the substrate beneath the clocking electrodes **195**, and beneath the signal sensing electrodes **194**. Walsh combination circuits **198** perform Walsh correlations on signals provided by the signal sensing electrodes **194**, thereby providing a plurality of envelope outputs. Then, a magnitude circuit and M-way compare circuit **200** provide a largest magnitude index signal **201** indicating which correlator of the Walsh combination circuits **198** yielded an envelope output having the largest magnitude. The largest magnitude index signal **201** is provided to a detect/data decode circuit **202** which performs data demodulation upon the signal.

If the PN-DSSS code is of a higher bandwidth than the CTD can support, the bandwidth of the received signal can be reduced before being processed by the CTD by removing the PN-DSSS modulation in a pre-correlator, after DS chip timing has been established during the synchronization cycle. The CTD can then performing Walsh correlations, data demodulation, and data decoding.

Establishing synchronization can also be performed in the CTD, either by a reconfiguration of the demodulation CTD channels, or by a separate CTD channel operating in parallel. If the same chip rate is preferred for both synchronization and demodulation, and if the preferred chip rate is higher than 25 MHz (for a 50 Msps device), parallel CCDs may be used, combined with a multiplexing structure to implement a matched filter.

Alternatively, the ACT technology could be used because of its higher inherent sampling rates. As another alternative, since there is no baud rate requirement for synchronization, a longer symbol can be used with a lower PN-DSSS code rate, thereby preserving processing gain.

The number of code chips in the matched filter can be further increased so as to provide a robust synchronization preamble. Precise timing can then be achieved in a sequential operation. In this way, for example, a spread spectrum code rate of 25 Mhz can be used for synchronization, while a Walsh chip rate of 25 Mhz can be used to encode data modulated by a 75 Mhz spread spectrum code that can be removed in the pre-correlator.

An important advantage of CTDs is that all associated support circuits and the storage cells can be integrated on the same device. Since modern CCDs use storage that resembles a dynamic RAM, CCD technology has benefitted directly from advances in packing density and speed of DRAM technology.

The magnitude and 8-way compare circuit **200** and the detection and data decode circuit **202**, (and optionally timing and frequency control loops), for example, are integratable directly on the device output, thereby greatly simplifying output processing.

Digital Implementation

The chip architecture is based on the basic cell and tree structure of FIGS. **22** and **23**. This architecture is efficiently achieved as in an integrated circuit (IC) or as a field programmable gate array (FPGA), since it is register-intensive and tree-like in form. A benefit of the tree architecture is that, even thought each stage includes the twice the amount of circuitry as its preceding stage, the later stage is only required to operate at half the speed of its preceding stage. The power distribution on the chip is thereby evenly distributed, and routing requirements of the most speed-intensive circuits are reduced. Consequently, the higher-speed input stages can use optimized routing. Also, the last stage, which operates relatively slowly and which requires many routing channels due to having the highest adder fanout, can be placed without constraint.

Communication over a non-Gaussian communications channel requires that a digital signal processor receive a wider input word than communication over a Gaussian communications channel. In a Gaussian channel, good signal normalization can be used to reduce the number of bits per input word to as low as one, thereby providing substantial hardware savings.

With reference to FIG. **19**, to accommodate non-Gaussian interference, and to reduce the accuracy required of the signal normalization circuits (e.g., automatic gain control), the embodiment of FIG. **19** uses 6 bit per word input samples **206** (5 bits plus a sign bit). A series of clock signal dividers **205** provides progressively slower clock signals. The input samples **206** are clocked into an input register **207**. The first stage add/sub module **208**, shown in detail in FIG. **19A**, operates on the six-bit two's-complement input **209** with sign extension to produce a seven bit output **211**.

To support 10 Mbps 8-ary signalling, the add/sub block **208** must operate at a 26.67 MHz clock rate. This is because a symbol rate of 3.333 Msps (million symbols per second) is required with eight Walsh chips/symbol (for 8-ary modulation) to achieve 10 Mbps with 3 bits/symbol.

Referring to FIG. **9A**, clock signal A is twice the speed of clock signal B, having been divided by a factor of two by a clock signal divider **205**. Consequently, an adder **210A** and a subtractor **210B** operate in parallel to provide a pair of outputs at a rate that is half the rate that input samples are presented to the add/subtract module **208**.

Clocking

After a pair of input samples are loaded into an input register **208A** of the first add/subtract module **208**, the results of adding and subtracting operations performed by modules **210A** and **210B**, respectively, are latched out upon the arrival of the next input sample. Thus, even though the add/subtract module **208** operates on a pair of samples at a time, the result must be ready in a single sample time. Similarly, the second stage Add/Sub blocks **212** operate on a pair of output samples **211** of the first stage Add/Sub block **208**. The results must be latched out to the next stage before next input samples arrive.

The third stage add/subtract modules **214** have been modified so that the output register **216** is placed after the 8-way compare **218**, thereby eliminating an extra frame delay, as well as eliminating M−1 registers (where M=8, in this example). The third stage add/subtract modules **214**, and the 8-way compare circuit **218**, operates at one fourth the input rate. If double buffering were used at the input to each stage, the computation rates would be halved, because an extra set of samples would be stored while awaiting processing.

There is typically some skew (delay) between the arrival of the clock signals at the latches of the inputs and the outputs of each stage. The difference between the latest arrival time of the input clock to the earliest arrival of the output clock, if positive, must be added to the maximum delay path of the logic to determine clocking rate. Excess delay may be added to the output clock to increase the speed, provided care is taken that minimum hold times are met for the shortest possible logic delay path.

The 8-way compare circuitry **218** is shown as an inverted binary tree structure having one half as many elements in each successive stage as in a previous stage. Since a single receiver channel is shown, the coherent carrier reference case is assumed, as shown in FIG. **14**. Thus, envelope detection is just a sign stripping function. First, the magnitude of each nine-bit envelope signal from the add/subtract modules **214** is determined in the sign-strip modules **220**. Then, magnitude comparisons are performed in pairwise fashion at each stage resulting in a single magnitude, of the largest byte, from a winning correlator. The value of the largest byte of each comparison is passed along to the next stage, while the index of the corresponding correlator is interpreted by the 7-to-3 decoder **222** as the orthogonal data demodulation result.

Architecture For Full I and Q Processing

In FIG. **20**, the pipelined architecture described in FIG. **19** is duplicated for the Q channel, wherein the circuitry for the I and Q channels are combined, with the 8-way compare circuitry, to provide full I and Q processing. FIG. **20** shows how quadrature-channel combining is performed, using the well-known approximation of adding the output of the largest value of the I **230** or Q **231** channels on each output pair to one half the output of the smaller value, in the combine I and Q blocks **232**. Therefore, the sign stripping, as performed by a sign strip module **220**, is still necessary on each channel.

According to the invention, the circuitry of FIG. **20** can be partitioned so as to provide a plurality of identical or nearly identical integrated circuits, the integrated circuits each being a cascadable structure suitable for combining with similar integrated circuits to form M-ary Walsh demodulators of arbitrary values of M.

The most direct way of accomplishing this partitioning, such that it becomes possible to partition the circuitry of FIG. **20** into FPGA chips, or into multiple custom or semicustom integrated circuits, is to place a single Walsh correlator on each chip. Additionally, the I and Q combining circuits are placed on a third chip that also includes 8-way compare circuitry. This approach to partitioning requires that each Walsh correlator chip include 64 output lines (8 bits by 8 channels), and that the combiner chip include 128 input lines. This amount of I/O is excessive, resulting in high cost and reduced reliability.

Referring to FIGS. **21A** and **21B**, the partitioning approach taught by the invention is to divide the circuitry into an upper segment **240**, shown in FIG. **21A**, and a lower segment **242**, shown in FIG. **21B**, keeping the I channel **244** and Q channel **246** of each segment together on the same chip. The upper and lower segments **240** and **242** are not connected until after the final comparison of the comparison tree **248**. The upper segment circuits **240** can be placed on one chip, and the lower segment circuits **242** can be placed on another chip. Only twenty four data lines are required to connect the two chips.

In the 8-ary circuitry shown in FIGS. **21A** and **21B**, after the first stage, seven lines in each of the I and Q channels are for interfacing to the other chip, and four complex correlators (**244, 246**) are included on a chip. The four I and four Q correlators (**244, 246**) on each chip are identical to those in FIG. **20**, but relate to only half the tree structure shown in FIG. **20**. After the four I and Q results are combined on each chip, they are reduced to a single largest value in a 4-way compare module **248**. This largest value (an 8-bit amplitude), along with two decoding lines, is exported to the other chip where it is compared to the result from the other half of the comparison tree, whereupon the largest of the two values is decoded. The result is a three bit word representing a demodulated symbol.

The circuitry may be further subdivided by parsing each section **240, 242** similarly into two smaller chips. Similarly,

the chips may be cascaded in the case of higher order alphabets, i.e, higher values of M. It is also possible to form a more symmetric partitioning by having one chip serve as a front-end source that feeds individual segments of the tree. For improved operating speed, necessary for higher alphabets, the number of signal lines between chips can be traded against speed of a speed-optimized front end. The symmetric front-end source is obtained by splitting the first stage Add/Sub block with the sum output feeding the upper segment and the difference output feeding the lower segment. A single input line can determine whether that stage is an adder or subtractor.

This approach allows use of multiple FPGA technology chips, or the use of multiple custom or semicustom integrated circuits, while maintaining modest size and interconnect complexity in each chip to increase yield and reliability. This approach allows a single chip of common circuits to be cascaded vertically and horizontally by a user to create arbitrarily large alphabets.

Other modifications and implementations will occur to those skilled in the art without departing from the spirit and the scope of the invention as claimed. Accordingly, the above description is not intended to limit the invention except as indicated in the following claims.

What is claimed is:

1. A method of transmitting data through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, the method comprising the following:

(A) providing data as a sequence of digital waveform symbols with said DSSS code and with phase rotations of differential quadrature phase shift keying (DQPSK), wherein each digital waveform symbol (a) represents N data bits and (b) is selected from a set of at least 2^N possible digital waveform symbols, wherein at least some of the digital waveform symbols are orthogonal to one another;

wherein (i) each digital waveform symbol of the set is unique from the others, (ii) the symbol uniqueness is determined by a unique pulse structure, (iii) the shortest pulse width of any of the digital waveform symbols in the set of digital waveform symbols defines a symbol modulation pulse width; and (iv) the DQPSK relates to the phase shift between each pair of sequentially neighboring digital waveform symbols in said sequence;

(B) modulating a carrier signal as a function of the digital waveform symbols with said DSSS code and with the DQPSK phase rotations so as to produce a modulated signal; and

(C) amplifying and transmitting a radio signal as a function of the modulated signal;

wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code.

2. The method according to claim 1, wherein the digital waveform symbols with said DSSS code without the DQPSK includes a quadrature component and an in-phase component.

3. The method according to claim 1, further including connecting the data device to a computer through an interface.

4. The method according to claim 1, wherein amplifying and transmitting a radio signal as a function of the modulated signal includes transmitting the radio signal through an antenna.

5. A method of transmitting data through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, the method comprising the following:

(A) providing data as a sequence of digital waveform symbols, wherein each digital waveform symbol (a) is selected from a set of at least 2^N digital waveform symbols, wherein at least some of the digital waveform symbols of the set are orthogonal to one another, and (b) represents N data bits, with each digital waveform symbol of the set being unique from the others, and (i) the symbol uniqueness being determined by a unique pulse structure and (ii) the shortest pulse width of any of the digital waveform symbols in the set of digital waveform symbols defining a symbol modulation pulse width;

(B) applying differential quadrature phase shift keying (DQPSK) to each pair of sequentially neighboring digital waveform symbols of the sequence so as to produce a digital waveform symbol with one of four possible DQPSK phase rotations;

(C) combining (i) said DSSS code with (ii) the digital waveform symbols with the DQPSK phase rotations;

(D) modulating a carrier signal as a function of digital waveform symbols with the DSSS code and with the DQPSK phase rotations so as to produce a modulated signal; and

(E) amplifying and transmitting a radio signal as a function of the modulated signal;

wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code.

6. The method according to claim 5, wherein each digital waveform symbol includes a quadrature component and an in-phase component.

7. The method according to claim 5, wherein the DSSS code includes a quadrature component and an in-phase component.

8. The method according to claim 7, wherein each digital waveform symbol includes a quadrature component and an in-phase component.

9. The method according to claim 5, further including connecting the data device to a computer through an interface.

10. The method according to claim 5, wherein amplifying and transmitting a radio signal as a function of the modulated signal includes transmitting the radio signal through an antenna.

11. A method of transmitting data through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, the method comprising the following:

(A) providing data as a sequence of digital waveform symbols with said DSSS code, wherein each digital waveform symbol with said DSSS code (a) is selected from a set of at least 2^N digital waveform symbols with said DSSS code, wherein at least some of the digital waveform symbols with said DSSS code of the set are orthogonal to one another, and (b) represents N data bits, with each digital waveform symbol of the set being unique from the others, and (i) the symbol uniqueness being determined by a unique pulse structure and (ii) the shortest pulse width of any of the digital waveform symbols in the set of digital waveform symbols, in the absence of said DSSS code, defining a symbol modulation pulse width;

(B) applying one of four possible phase rotations of differential quadrature phase shift keying (DQPSK) to each pair of sequentially neighboring digital waveform symbols of the sequence with said DSSS code so as to produce a sequence of digital waveform symbols with said DSSS code and with DQPSK phase rotations;

(C) modulating a carrier signal as a function of digital waveform symbols with said DSSS code and with said DQPSK phase rotations so as to produce a modulated signal; and

(D) amplifying and transmitting a radio signal as a function of the modulated signal;

wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code.

12. The method according to claim **11**, wherein each digital waveform symbol with said DSSS code includes an in-phase component and a quadrature component.

13. The method according to claim **11**, further including connecting the data device to a computer through an interface.

14. The method according to claim **11**, wherein amplifying and transmitting a radio signal as a function of the modulated signal includes transmitting the radio signal through an antenna.

15. A method of transmitting data through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, the method comprising the following:

(A) providing data as a sequence of digital waveform symbols with any one of four differential quadrature phase shift keying (DQPSK) phase rotations between each pair of sequentially neighboring digital waveform symbols in said sequence, wherein each digital waveform symbol (a) is selected from a set of at least 2^N digital waveform symbols, at least some of the digital waveform symbols of the set being orthogonal to one another, and (b) represents N data bits, with each digital waveform symbol of the set being unique from the others, and (i) the symbol uniqueness being determined by a unique pulse structure and (ii) the shortest pulse width of the any of the digital waveform symbols in the set of digital waveform symbols defining a symbol modulation pulse width; and

(B) combining said DSSS code with the digital waveform symbols with said DQPSK phase rotations;

(C) modulating a carrier signal as a function of the digital waveform symbols with the DQPSK phase rotations and with the DSSS code so as to produce a modulated signal; and

(D) amplifying and transmitting a radio signal as a function of the modulated signal;

wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code.

16. The method according to claim **15**, wherein the digital waveform symbols without the DQPSK phase rotations each includes a quadrature component and an in-phase component.

17. The method according to claim **15**, wherein the DSSS code includes a quadrature component and an in-phase component.

18. The method according to claim **17**, wherein each digital waveform symbol without the DQPSK phase rotations includes a quadrature component and an in-phase component.

19. The method according to claim **15**, further including connecting the data device to a computer through an interface.

20. The method according to claim **15**, wherein amplifying and transmitting a radio signal as a function of the modulated signal includes transmitting the radio signal through an antenna.

21. A method of transmitting data through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, the method comprising the following:

(A) providing data as a sequence of digital waveform symbols, wherein each digital waveform symbol (a) occurs during the time of a symbol period, and (b) is selected from a set of at least 2^N digital waveform symbols, wherein at least some of the digital waveform symbols of the set are orthogonal to one another, and (c) represents N data bits, with each digital waveform symbol of the set being unique from the others, and (i) the symbol uniqueness being determined by a unique pulse structure and (ii) the shortest pulse width of any of the digital waveform symbols in the set of digital waveform symbols defining a symbol modulation pulse width;

(B) differential quadrature phase shift keying (DQPSK) on the DSSS code in each pair of sequentially neighboring symbol periods;

(C) combining the sequence of digital waveform symbols with DSSS code after said differential quadrature phase shift keying (DQPSK) in each pair of sequentially neighboring symbol periods so as to produce a sequence of digital waveform symbols with said DSSS code and with DQPSK phase rotations;

(D) modulating a carrier signal as a function of the digital waveform symbols with the DSSS code and with the DQPSK phase rotations so as to produce a modulated signal; and

(E) amplifying and transmitting a radio signal as a function of the modulated signal;

wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code.

22. The method according to claim 21, wherein each digital waveform symbol includes a quadrature component and an in-phase component.

23. The method according to claim 21, wherein the DSSS code without DQPSK on sequential symbol periods includes a quadrature component and an in-phase component.

24. The method according to claim 21, further including connecting the data device to a computer through an interface.

25. The method according to claim 21, wherein amplifying and transmitting a radio signal as a function of the modulated signal includes transmitting the radio signal through an antenna.

26. A method of receiving data transmitted through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, wherein data is transmitted as a sequence of digital waveform symbols with said DSSS code and with phase rotations of differential quadrature phase shift keying (DQPSK), wherein each of the digital waveform symbols is representative of N bits of data and is selected from a set of at least 2^N possible digital waveform symbols, at least some of the digital waveform symbols being orthogonal to one another;

wherein (i) each digital waveform symbol of the set is unique from the others, (ii) the symbol uniqueness is determined by a unique pulse structure, (iii) the shortest pulse width of any of the digital waveform symbols in the set of digital waveform symbols defines a symbol modulation pulse width; and (iv) the DQPSK relates to the phase shift between each pair of sequentially neighboring digital waveform symbols in said transmitted sequence; and wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code; the method comprising the following:

receiving a radio signal from the common radio communication channel so as to provide an incoming signal as a function of the data transmitted through the communication channel and received by the data device;

correlating the incoming signal with said set of digital waveform symbols with said DSSS code so as to provide a first sequence of data bits representing a sequence of most likely transmitted digital waveform symbols;

providing a second sequence of data bits as a function of the differential phase shift between each pair of sequentially neighboring digital waveform symbols with said DSSS code in said transmitted sequence; and

converting the first and second sequence of data bits into a digital data bit sequence.

27. The method of claim 26, wherein each digital waveform symbol with DSSS code of said set includes an in-phase component and a quadrature component, and wherein the step of correlating the incoming signal includes correlating the incoming signal with the in-phase component and quadrature component of each digital waveform symbol with DSSS code of said set so as to provide a sequence of data bits representing a sequence of most likely transmitted complex digital waveform symbols.

28. The method of claim 26, wherein the step of receiving includes using an antenna to receive a radio signal from the common radio communication channel from any other data device connected to the network.

29. The method of claim 26, further including connecting the data device to a computer through a computer interface.

30. The method of claim 26, further including connecting the data device to a data interface.

31. The method of claim 26, further including connecting the data device to a printer.

32. The method of claim 26, further including connecting the data device to a mass data storage device.

33. The method of claim 32, wherein the mass data storage device is a file server.

34. The method of claim 26, further including connecting the data device to an antenna, band pass filter and a down converting stage.

35. A method of receiving data transmitted through a common radio communications channel forming a wireless connection between any two data devices of a local area network comprising a plurality of such data devices, wherein each data device (i) uses the same direct-sequence spread spectrum (DSSS) code of a known chip width and (ii) uses spread spectrum processing gain so as to suppress unknown interference signals and unknown multipath signals, wherein data is transmitted as a sequence of digital waveform symbols with said DSSS code and with phase rotations of differential quadrature phase shift keying (DQPSK), wherein each of the digital waveform symbols is representative of N bits of data and is selected from a set of at least 2^N possible digital waveform symbols, at least some of the digital waveform symbols being orthogonal to one another;

wherein (i) each digital waveform symbol of the set is unique from the others, (ii) the symbol uniqueness is determined by a unique pulse structure, (iii) the shortest pulse width of any of the digital waveform symbols in the set of digital waveform symbols defines a symbol modulation pulse width; and (iv) the DQPSK relates to the phase shift between each pair of sequentially neighboring digital waveform symbols in said transmitted sequence; and wherein the known chip width of said DSSS code is equal to the symbol modulation pulse width of the set of digital waveform symbols in the absence of the DSSS code; the method comprising the following:

receiving a radio signal from the common radio communication channel so as to provide an incoming signal as a function of the data transmitted through the communication channel and received by the data device; and

performing each of the following: (i) removing the DSSS code, (ii) correlating with digital waveform symbols of the set, and (iii) determining the phase shift between each pair of sequentially neighboring digital waveform symbols in said transmitted sequence, so as to provide a digital data bit sequence as a function of the most likely transmitted digital waveform symbols and the phase shift between each pair of sequentially neighboring digital waveform symbols in said transmitted sequence.

36. The method of claim 35, wherein each digital waveform symbol of said set includes an in-phase component and a quadrature component, and wherein the step of correlating with digital waveform symbols of the set includes correlating with the in-phase component and quadrature component of each digital waveform symbol of said set so as to provide a sequence of data bits representing a sequence of most likely transmitted complex digital waveform symbols.

37. The method of claim 35, wherein the step of receiving includes using an antenna to receive a radio signal from the common radio communication channel from any other data device connected to the network.

38. The method of claim 35, further including connecting the data device to a computer through a computer interface.

39. The method of claim 35, further including connecting the data device to a data interface.

40. The method of claim 35, further including connecting the data device to a printer.

41. The method of claim 35, further including connecting the data device to a mass data storage device.

42. The method of claim 41, wherein the mass data storage device is a file server.

43. The method of claim 35, further including connecting the data device to an antenna, band pass filter and a down converting stage.

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